HELSINKI UNIVERSITY OF TECHNOLOGY
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Deep Reactive Ion Etching for Microfluidic Structures

Thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Engineering.

Espoo, 10. February 2006

Supervisor:

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Preface

This master's thesis was prepared at the Microelectronic Centre of the Helsinki University of Technology between May 2005 and February 2006. The subject was chosen because of my interest in processing of silicon and because new DRIE equipment was recently acquired to the clean room of the Microelectronic Centre.

I would like to thank Microelectronic Centre for giving me the opportunity to do this thesis. I would also like to thank professor Ilkka Tittonen for supervising and doctor Sami Franssila for directing this thesis. Their instructions and advices were priceless. Thanks goes also to the staff of Viikki Drug Discovery Technology Centre, University of Helsinki. Without their help and knowledge DIOS experiments would not have been finished. Big thanks also to the personnel of Microelectronic Centre for inspiring atmosphere.

Special thanks goes to my parents Annukka and Jukka for their support.

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Lauri Sainiemi

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The first part of this master's thesis focuses on characterizing cryogenic deep reactive ion etching (DRIE) process of silicon with high density SF_6/O_2 plasma. The relationship between equipment parameters and etch responces was explored. As a result, the maximum etch rate could be raised from 4 μm/min to 7,6 μm/min.

The second part of the thesis concentrates on utilizing cryogenic DRIE for the fabrication of microfluidic devices. The lidless capillary filling chip was designed, fabricated and tested. Experimets with fluorescent markers show that high aspect-ratio microposts on the bottom of the channel initiate capillary flow.

Desorption / ionization on silicon (DIOS) experiments were done with porous silicon and black silicon sample plates and the results were compared with each other. The easy fabrication process of black silicon makes it attractive material in DIOS applications.

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Tämän diplomityön ensimmäinen osa keskittyy kylmässä tapahtuvan, tiheää SF_6/O_2 plasmaa käyttävän, piin syvän reaktiivisen ionietsaus prosessin karakterisointiin. Työssä tutkittiin laiteparametrien vaikutsta etsaustulokseen. Tutkimuksen tulopksena suurin saavutettu etsausnopeus nousi 4:stä μm/min 7,6:iin μm/min.

Diplomityön toisessa osassa keskitytään hyödyntämään syvä ionietsaus prosessia mikrofluidististen laitteiden valmistuksessa. Kanneton kapillaarivoimilla täyttyvä kanava suunniteltiin, valmistettiin ja testattiin. Kokeet fluoresoivilla merkkiaineilla osoittivat, että korkean aspektisutheen mikropilarit kanavan pohjalla saavat aikaan kapillaarivirtauksen.

DIOS kokeita tehtiin sekä mustasta että huokoisesta piistä valmistetuista näytealustoista ja tuloksia verrattiin toisiinsa. Mustan piin helppo valmistusprosessi tekee siitä houkuttelevan materiaalin DIOS sovelluksiin.

Abbreviations

ARDE	Aspect ratio dependent etching
BHF	Buffered hydrogen fluoride
BS	Black silicon
CCP	Capacitively coupled plasma
CE	Capillary electrophoresis
C_4F_8	Octofluoro cyclobutane
COMOSS	Collocated monolithic support structures
DI	De-ionized
DIOS	Desorption / ionization on silicon
DRIE	Deep reactive ion etching
DSP	Double side polished
ER	Etch rate
FFE	Free flow electrophoresis
HAR	High aspect ratio
HBr	Hydrogen bromide
IC	Integrated circuits
ICP	Inductively coupled plasma
LC	Liquid chromatography
LOC	Lab-on-a-chip
MALDI	matrix-assisted laser desorption ionization
MEMS	Microelectromechanical systems
MS	Mass spectrometry
PR	Photoresist
RIE	Reactive ion etching
sccm	Standard cubic centimetre
SEM	Scanning electron microscope
SF_6	Sulphur hexafluoride
SiF_4	Silicon tetrafluoride
SiO_2	Silicon dioxide
SiO_xF_y	Silicon oxyfluoride
SSP	Single side polished
TAS	Total analysis systems

TMAH	Tetramethyl ammonium hydroxide
TLC	Thin layer chromatography
μTAS	Miniaturized total analysis systems

1 Introduction

Silicon is the second most common element in the Earth's crust and by far the most common material used in microfabrication. Integrated circuits (IC) industry relies mostly on silicon because of its electrical properties. Silicon has also many other excellent qualities; it is mechanically as strong as steel; it is available in different shapes and sizes and it is also quite cheap material. Still, the main reason why the microtechnology mostly relies on silicon is the fact that IC industry has already developed sophisticated fabrication tools and methods to machine silicon.

Development of mircofluidic analysis systems started in early 1990's. Most of the fabrication processes are still the same as in IC fabrication, but some of the requirements are different. In many microfluidic devices several hundreds of micrometers deep structures are desirable while in IC processes only a few micrometers is enough. In order to create deep and narrow trenches deep reactive ion etching (DRIE) has been developed.

The focus of this thesis is to study cryogenic DRIE process and utilize it in the fabrication of microfluidic devices. In chapter 2, the most common microfluidic applications where DRIE is needed are introduced. The theory and development of cryogenic DRIE are reviewed in chapter 3. Characterization of DRIE equipment and comparison of experimental results with the theory, are presented in chapters 4-8. The fabrication process of capillary filling chip is discussed in chapter 9. The results of the experiments are also presented. In chapter 10, the suitability of black silicon (BS) in desorption / ionization on silicon mass spectrometry (DIOS-MS) is demonstrated. The most important results and the future prospects of the thesis are concluded in chapter 11.

2 High-aspect-ratio structures in microfluidics

In this chapter the concept of microfluidics is introduced and a few microfluidic applications where high aspect ratio (HAR) structures are needed are presented. If height-to-width ratio is more than 2:1 it can be considered as a HAR structure. Also the benefits and downsides of these miniaturized fluidic systems are considered.

2.1 Introduction to microfluidics

Analytical chemistry is important field to microfluidic systems. Analytical chemistry tries to find out what materials some sample contains; what are the quantities of different components in the sample and what are the forms of the existing components. This kind analysis process requires many steps that include inconvenient manual sample transportation from one place to other [1].

The concept of total chemical analysis system (TAS) was presented in early 1980s and its purpose was to help the work of analytical chemists. The main idea was to incorporate analytical procedures into flowsystems. Fluid streams replaced the sample transportation with human hands between different process steps. The goal was to create an analysis system that was capable of analyzing the sample in the field. Unfortunately early total analysis systems were big and heavy and therefore awkward [1].

The concept of miniaturized total analysis systems (μTAS) was first introduced by Manz and his co-workers in 1990 [2]. μTAS is a smaller version of original TAS where big tubes are replaced with small microchannels. Fabrication of μTAS is fairly easy because it is typically done on silicon wafer and standard process steps are utilized. Nowadays DRIE plays a big role in fabrication process.

Miniaturized total analysis systems have many obvious benefits when comparing them to TAS. The small size of μTAS eases to transport of these systems. Cross section diameters of microchannels are usually order of tens of micrometers. Therefore sample volumes needed are small. Because of short distances analysis process is also quick. These small systems have practically always large surface-to-

volume ratio that ensures good heat dissipation which enables the use high electrical fields. The scaling of the surface-to-volume ratio is easy to understand with a simple calculation. The ratio between the surface area and volume of circular channel is presented in equation {1}. In microsystems the radius of the channel r is very small and therefore the ratio is big. Parameter h is the length of the channel.

$$\frac{A}{V} = \frac{2\pi rh}{\pi r^2 h} = \frac{2}{r} \qquad \{1\}$$

Power consumption of μTAS is small. Standard microfabrication methods also make mass production possible and therefore these mircodevices are relatively cheap. Still, it must be kept in mind that small microfluidic chips are often connected to large machines such as mass spectrometers that consume lot of power. Also fabrication of μTAS can be power consuming. μTAS can also be called as microfluidic system and lab-on-a-chip (LOC) [1, 3, 4, 5, 6, 7].

Unfortunately small size also brings new problems. If concentration of sample solution is small there might be just a few molecules of interest inside the small sample volume. Detection of a single molecule is almost impossible. Miniaturized analysis systems have also some handling losses like adsorption on the sidewalls. Small channels also clog easily, especially when using real samples that may contain particles, bubbles, cells or other biological objects. Connection of these micro devices to macro world can also be tricky [1].

2.2 Liquid chromatography (LC)

2.2.1 Theory of LC

Most real samples are complex and they consist of many different compounds. In many situations the separation of different components is needed before detection. Chromatography is one way to do it. It is based on the fact that different materials have different affinities for stationary and mobile phases. The basic idea of chromatography is shown in Figure 1. Chemistry behind the chromatography is not in a focus of this thesis, and the reader is referred to [1, 8].

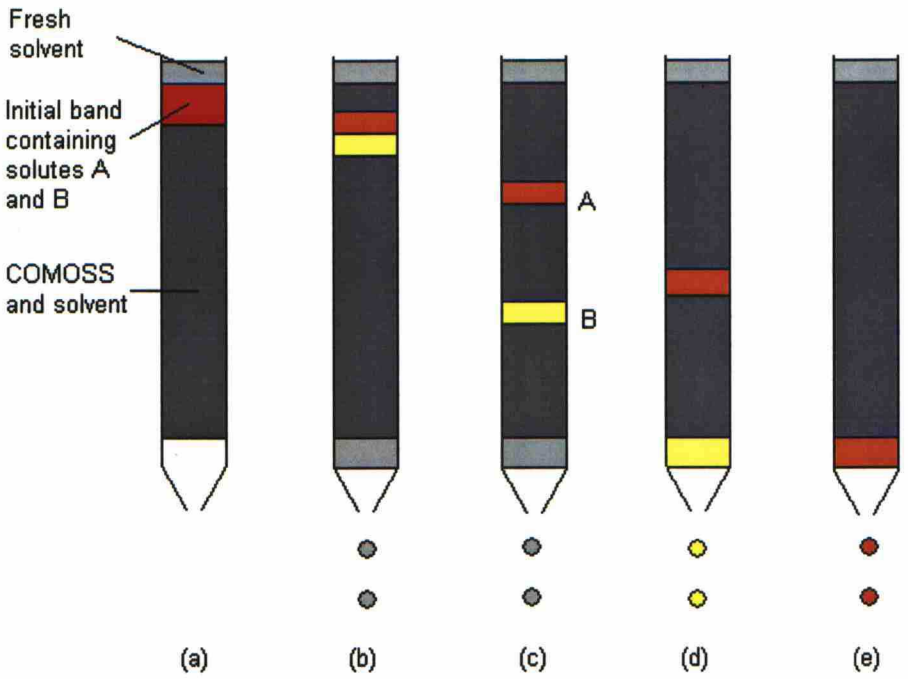


Figure 1. Shematic representation of a chromatographic separation. Solute A remains longer in the spearation channel than solute B because it has grater affinity to stationary phase than solute B. (a) Separation process starts. Solvent and sample that contains solutes A and B are fed into channel. (b) Solutes A and B start to separate from etch other. (c) Solutes A and B are clearly separated. (d) Solute B emerges. (e) Solute A emerges [9]. When the solute emerges it can be ionized and detected with mass spectrometer.

2.2.2 Liquid chromatography on chip

For more than half a century, tubular LC channels have been prepared by packing them with small porous particles that support the stationary phase. The interfacial area between the stationary and the mobile phase becomes large because of these particles. The large surface area results in intensive the reaction between the sample and stationary phase is. Unfortunately packing particles to rectangular microchannels is not easy. Nonuniformity of particles is a common problem and packing is especially difficult to complex channel networks [8, 10, 11].

Another possibility to create high surface-to-volume ratio channels was introduced by Regnier and his group [10]. They micromachined so called collocated monolithic support structures (COMOSS) inside the channel with help of conventional lithography (Figure 2). This approach offers many benefits. The fabrication method circumvents the need of particle packing; the location of support structures can be

defined accurately; channels and support structures are defined in the single lithography step.

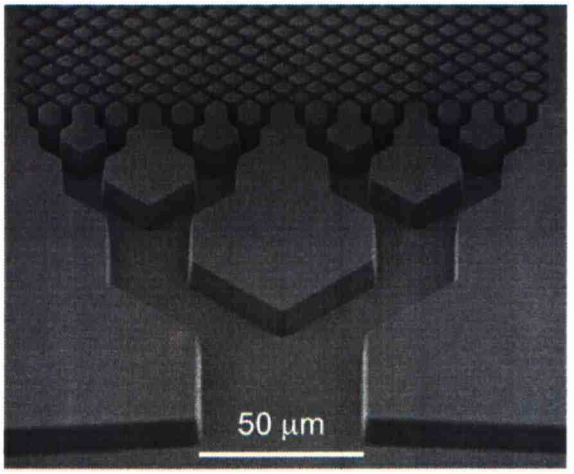


Figure 2. SEM picture of COMOSS. The pillars are perfecty arranged inside the channel [10]

Later it was also proven that efficiency of pressure driven liquid chromatography system could be improved when using micro-pillar structured channels because perfectly ordered support structures eliminate the possibility of variations in flow path length and local velocity. Considering dispersion, the positioning of the pillar row closest the sidewall is crucial. If the distance is too small the flow rate of the sample is slower at the sidewall region. In contrast, if the distance is too large species near the sidewall run ahead. Both of these scenarios result in band broadening. When the location of the first pillar row is chosen correctly, the sample propagates with constant velocity and band broadening is at its minimum (Figure 3). These simulations and experiments were made in pressure driven circumstances [11, 12].

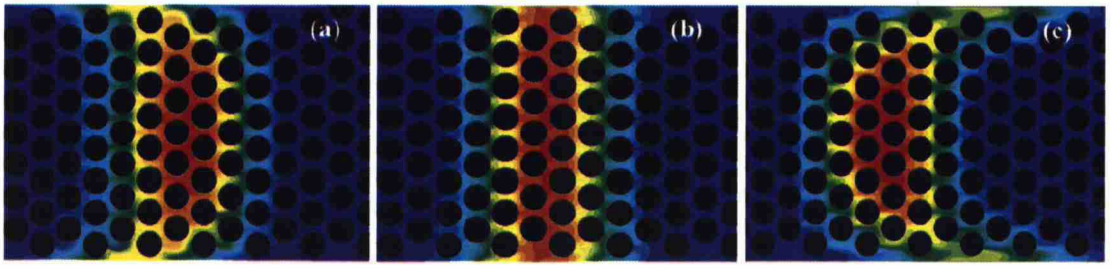


Figure 3. The effect of the pillar row closest the sidewall. Simulated concentration of the sample inside the pillar channel 0,1 s after injection. (a) The first pillar row is too close to the sidewall. (b) Ideal situation. (c) The first pillar row is too far away from the sidewall [11].

2.3 Free flow electrophoresis (FFE)

FFE is a separation technique that utilizes electric field perpendicular to pressure driven sample flow. It is capable of separating only charged particles. Schematic picture of the FFE chip is presented in Figure 4. The sample is inserted to chip continuously at the sample inlet and it is driven through the separation bed by the pressure-driven flow of the carrier liquid. Between the separation and side beds there are V-groove arrays that act as membranes. Electrodes are placed inside the side beds and electrical field is applied across the separation bed. Therefore charged species deflect from the direction of the flow. The deflection angle is dependent on charge-to-mass ratio of the ions, the strength of the electric field, the flow rate of carrier solution and the electrophoretic mobility of the sample species. At the end of the separation bed there are many outlets that collects individual sample components for further analysis [4, 13].

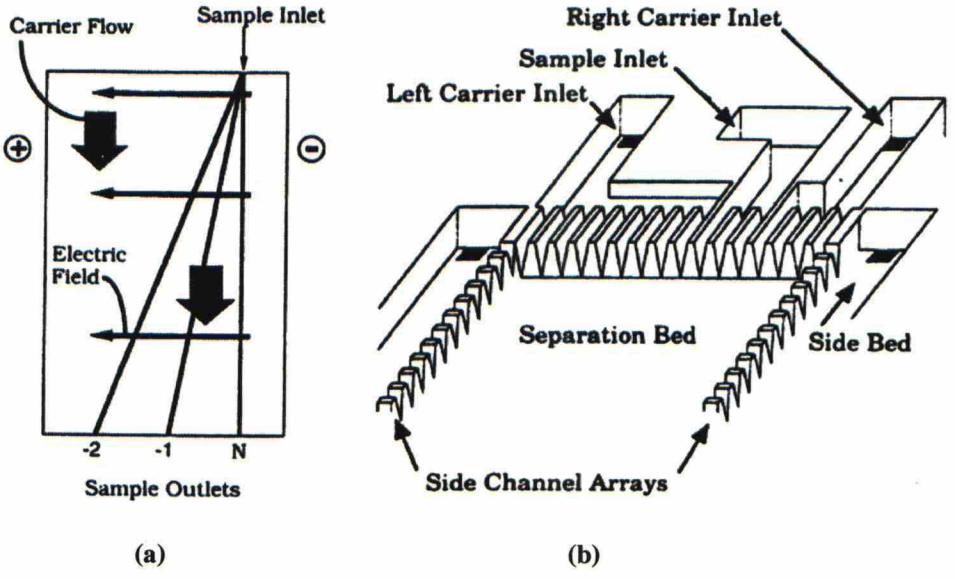


Figure 4. (a) The working principle of FFE. The charged particles of the sample deflect because of the elecric field perpendicular to flow [13]. (b) A schematic picture of the inlet region of the silicon FFE system [13].

2.4 Capillary filling

Reliable capillary filling is often needed in microfluidic devices. Liquid moves inside the capillary without external force because of the capillary pressure. It drives the liquid through the channel like shown in Figure 5.

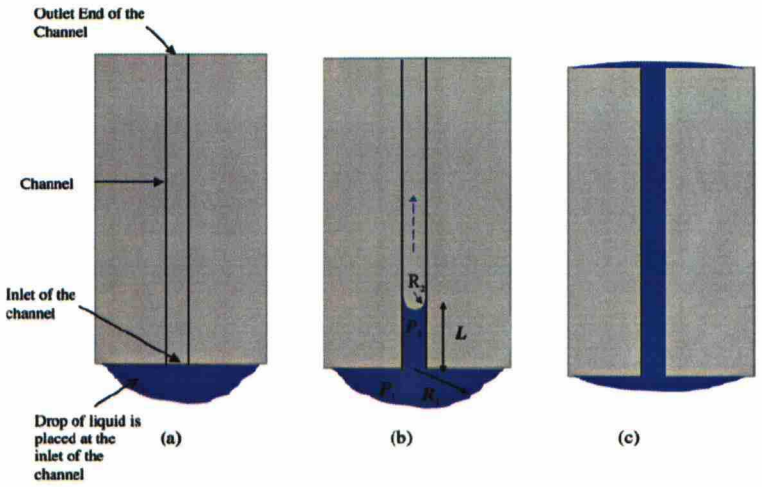


Figure 5. The theory of pressure driven capillary flow inside the microchannel. At the picture the channel that is open on both ends is depicted. (a) A sample drop is placed at the inlet of the channel. (b) The shapes of the propagating (R_2) and receding (R_1) menisci are different. That causes the pressure difference inside the capillary that transports the liquid forward. (c) When the sample has flown through the channel and rechases the outlet, the radii $R_1 = R_2$ and there is no pressure difference anymore. The sample flow stops [14].

In small channels the capillary pressure is high because differential pressure inside the channel can be approximated with equation

$$\Delta P = \frac{\sigma}{R_2} = 2\sigma * \cos\theta * (\frac{1}{d} + \frac{1}{w}) \ , \qquad \{2\}$$

where σ the surface tension of the sample, R_2 is the radius of propagating meniscus, θ contact angle, d is the height of the channel and w the width of the channel. The contact angle describes how hydrophilic or hydrophobic the sample is. The liquid is hydrophobic if $\theta \geq 90°$ and therefore there is no capillary flow [14, 15].

The theory described above applies only to the capillaries but it was demonstrated that capillary filling could be achieved also in channels that do not have a lid [16]. If there are HAR posts close to each other inside the channel, it creates micropillar driven capillary flow. The physics behind the phenomenon is the same as in capillaries. The sample application and detection is much easier on lidless channels. Also the fabrication of lidless channels is easier than fabrication of a capillary. Lidless channels are fabricated and tested in the experimental part of this thesis.

2.5 Passive valve for microfluidics

As discussed in previous chapter, capillary forces move the sample trough capillary without external forces. The drawback of capillary filling is that flow cannot be controlled directly. Still, by designing the capillary network properly passive valves can be created [17].

In the Figure 6 the operation of passive valve is demonstrated. The sample is driven through the channel by the capillary force until it stops to the geometrical valves. The operation of geometrical valve is based on the fact that an abrupt change of the geometry of the hydrophilic microchannel stops the flow of the sample. The sample that flows through the trigger channel opens the geometrical valves. This is an easy way to create programmable valves without any active elements. The length of the trigger channel defines the time that the sample is stopped at geometrical valves. Flow channels and geometrical valves can be defined accurately with DRIE [17].

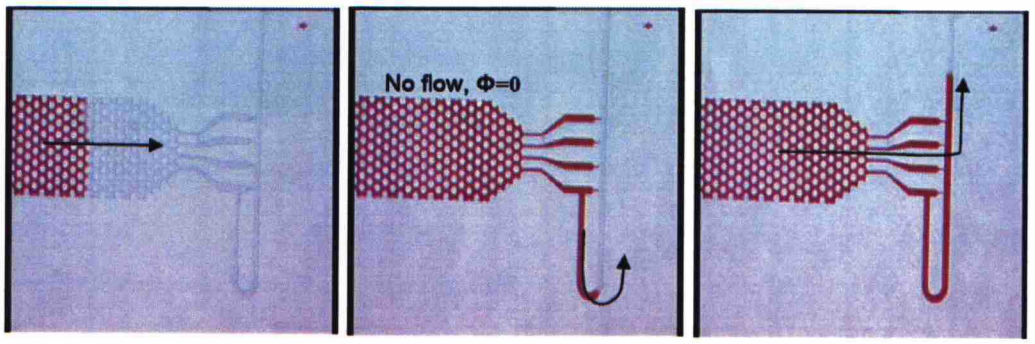


Figure 6. Passive valve for microfluidic devices. (a) Capillary force drives the sample through the channel. (b) Geometrical valves stop the sample flow, but the sample in trigger channel keeps flowing. (c) Geometrical valves are opened [17].

2.6 Microchannels without bonding

In some microfluidic applications strong interactions between sidewalls and sample fluid are desirable. Therefore channels that have high surface-to-volume ratio are needed. Normally bonding of a lid is the last process step when fabricating HAR channels. This process step makes harder to integrate other micromachined devices on the wafer. On the other hand, conventional surface micromachined channels have

inconvenient step of etching sacrificial layer from the channel. This often limits the length and the quality of the channel [18].

HAR microfluidic channels can be fabricated to silicon wafer without the bonding and sacrificial etching steps. The process has two steps: first DRIE is performed and then the etched channel is embedded with conformal parylene deposition that also encloses the channel (see Figure 7). Controlling the undercutting accurately is crucial in this fabrication approach. Undercutting makes possible to form closed channels with deposition step. SEM pictures of fabricated chennels are shown in the Figure 8 [18].

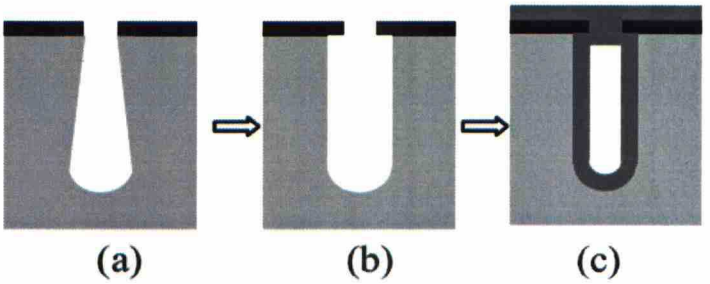


Figure 7. Fabrication of parylene coated HAR channels. (a) and (b) DRIE with suitable undercutting. (c) Parylene deposition that encloses the channel [18].

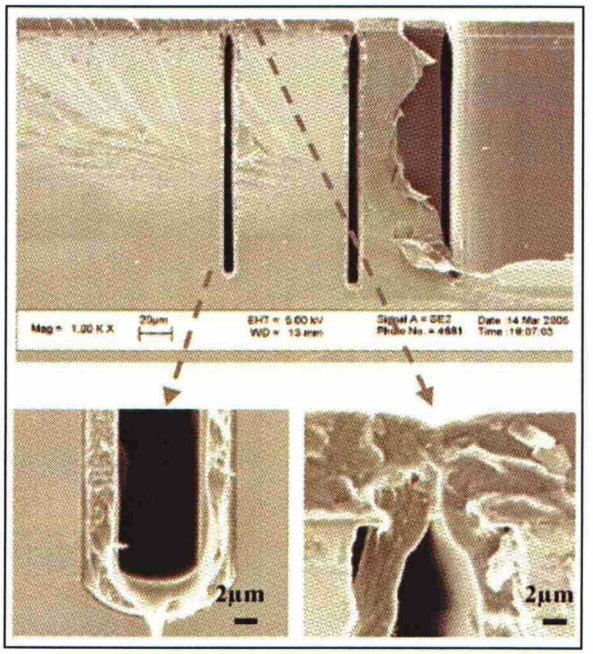


Figure 8. SEM images of fabricated HAR embedded parylene channels and their close-up views [18].

Tjerkstra and his co-workers [19] used same kind of approach in fabrication of nitride-coated tubular channel (see Figure 9). The process started with DRIE of silicon. 100 μm deep and only a few microns wide trenches are etched. Next, nitride layer is deposited to the wafer and it is removed from the bottom of the trenches with regular RIE. The silicon nitride layer on the surface of the wafer is thicker than the layer on the trench bottom. Therefore silicon is revealed only from the bottom of the trenches. Next, isotropical wet etching is performed to realize the channels. Only bare silicon surface is etched. Then nitride mask is removed and new thick layer is deposited to coat the capillaries and to enclose the channels. The thickness of the last layer has to be so big that it encloses the DRIE etched trench. Thermal silicon oxide, LPCVD nitride and polysilicon are suitable materials for last deposition.

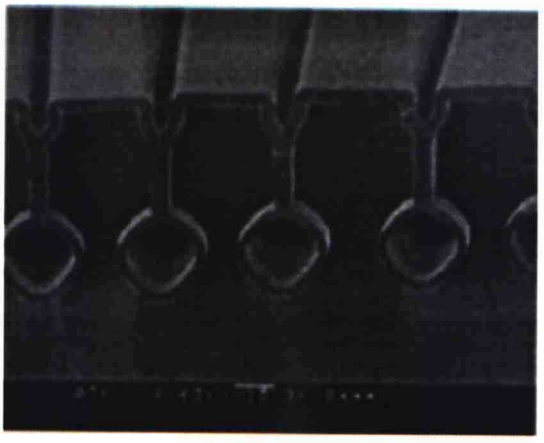


Figure 9. SEM image of the nitride-coated tubular capillaries [20].

2.7 Flow-through filter for beads

Microspheres, also known as beads, are nowadays commonly used in microfluidic systems. They are especially important in many medical applications. Material selection of the beads is very large and sizes go down to a few nanometers. The surface chemistry of the beads can be easily modified by attaching functional groups on them [21].

Traditionally beads have been made from magnetic iron oxide and they have been moved with the help of magnetic fields, but this can be inconvenient and may require integration of magnetic components on chip. Therefore flow-through filter for beads was invented. This approach is applicable to non-magnetic beads as well. One filter

design is presented in Figure 10. The filter utilizes HAR silicon pillars that let the fluid flow through but stops the beads. If the function of the beads is to generate a chemical reaction, this design ensures that reaction takes place at the specific location. Non-magnetic beads are usually made from polystyrene.

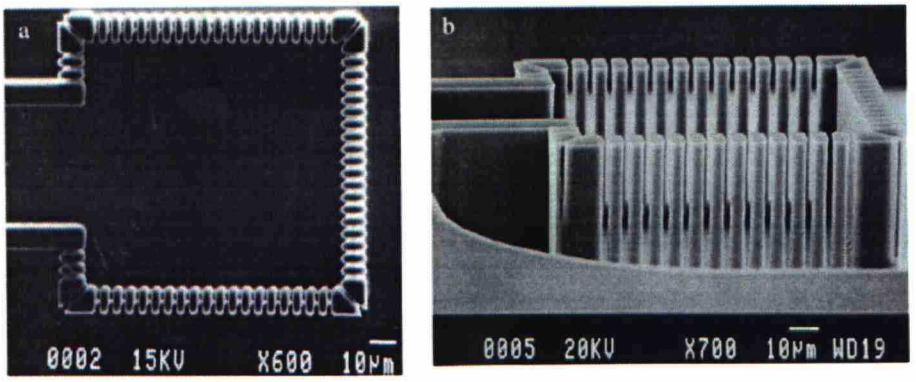
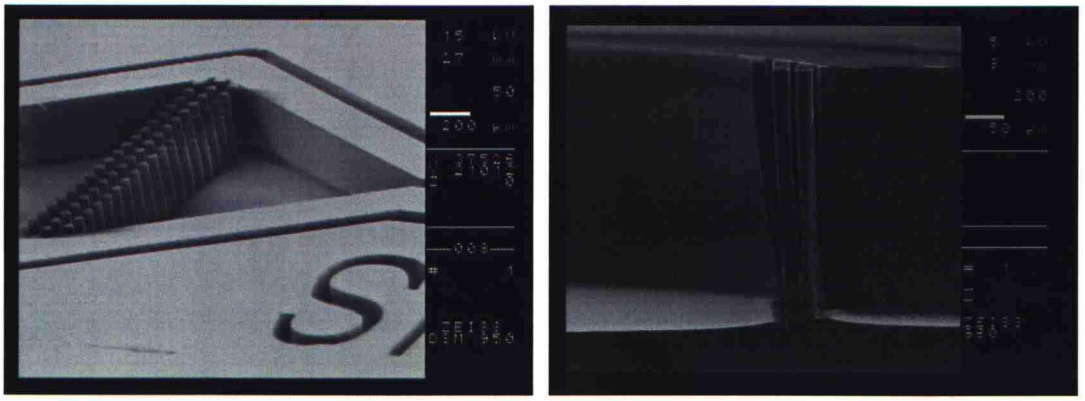


Figure 10. SEM images of the reaction chamber. (a) Top view. (b) Tilted side view [21].

Another kind of bead filter design is presented in Figure 11. Identiacal versions were made of both SU-8 photopolymer and silicon. The fabrication of silicon version is as easy as fabrication of polymer version when utilizing DRIE. Because silicon has superior mechanical properties compared to SU-8 and it is easy to integrate other components to silicon chip, the silicon version of the filter has considerably larger range of applications than SU-8 version.



(a) **(b)**

Figure 11. Another kind of filter design. (a) A flow-through filter. The filter is fabricated from the SU-8 polymer. Photo courtesy to Santeri Tuomikoski, Helsinki University of Technology. (b) A side view of the same filter fabricated from silicon. Photo courtesy Kai Kolari, VTT Information Technology.

2.8 Desorption / ionization on silicon mass spectrometry (DIOS-MS)

DIOS is matrix-free strategy for mass spectrometry. Analyte is usually dissolved in water or methanol and sample volume of approximately 1 µl is applied on round 1 mm porous silicon spot that is 1 µm thick. The mass spectrum is acquired by irradiating the sample with pulsed laser that ionizes the sample molecules and desorbs them. The ions are accelerated in high electric field and analyzed with mass spectrometer. The reason why ionization occurs is not well understood but it is believed that porous silicon absorbs laser radiation efficiently and enough energy is transferred from surface to analyte molecules, so that ionization and desorption occur. Since matrix compound is not needed, the background of mass spectrum is low. The working principle of DIOS-MS is presented in Figure 12 [22, 23].

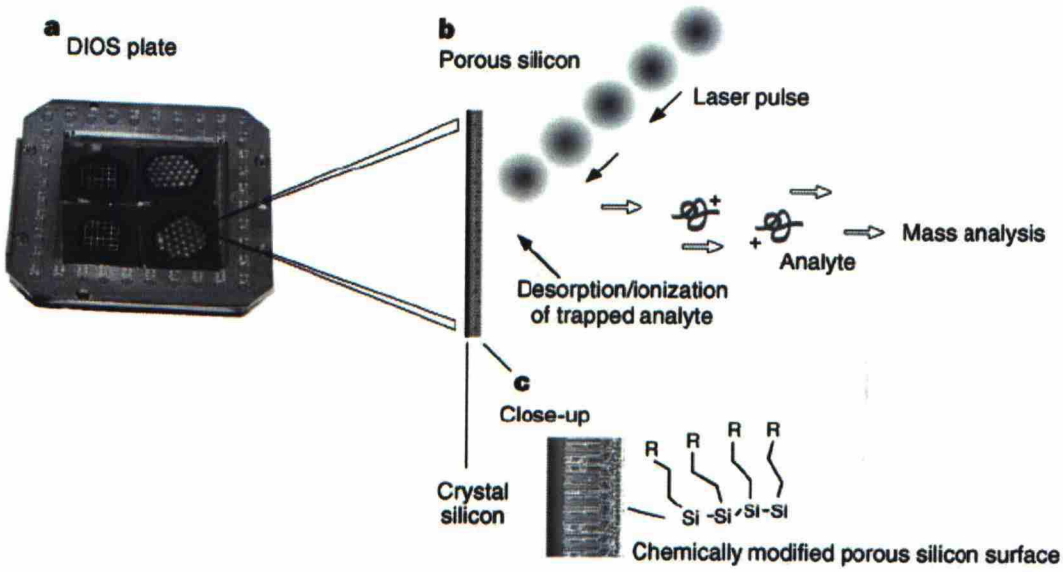


Figure 12. The working principle of DIOS-MS. (a) porous silicon DIOS plates are attached to target. (b) porous silicon plate where sample has been applied is irradiated with laser pulse and analyte molecules are desobed and inoized. (c) Close-up view of chemically stabilized porous silicon surface [22].

The sample is applied on porous silicon because of its the high surface area (see Figure 13). Therefore it traps the analyte molecules efficiently. Porous silicon also has high absorptivity in the ultraviolet range and therefore it is easy to bring energy to porous silicon surface with laser.

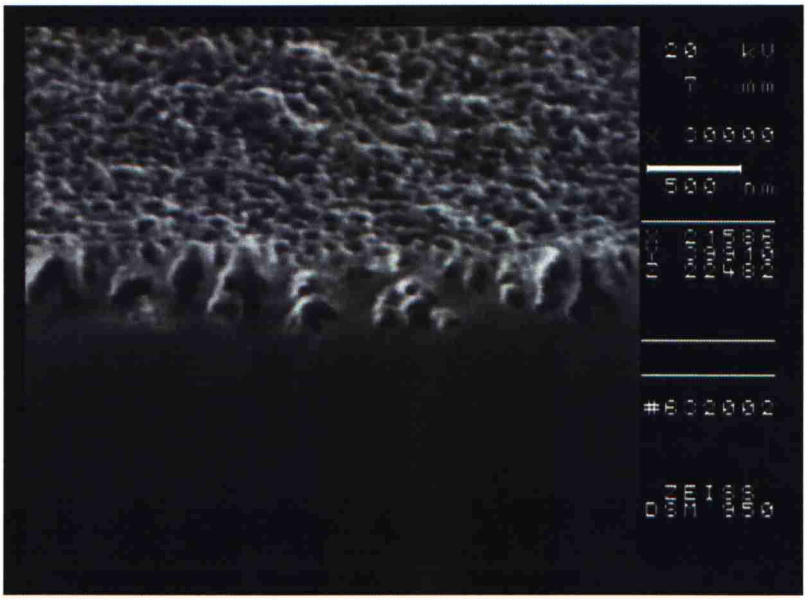


Figure 13. SEM picture of cross-section of porous silicon. Surface area of porous silicon is large. Picture courtesy Kestutis Grigoras, Helsinki University of Technology.

In chapter 10 of this thesis, it is demonstrated that porous silicon can be replaced with same kind of material called black silicon that is fabricated in cryogenic DRIE process (see Figure 43).

DIOS-MS is has many potential applications because porous silicon and black silicon are quite cheap materials and they can easily be integrated to silicon chips. At the time DIOS technique is used particularly in the analysis of small drug molecules [23].

3 DRIE at cryogenic temperatures

Fabrication of microelectromechanical system (MEMS) requires etching methods that provide high etch rate (ER), good selectivity and high aspect ratios. At the same time the profile control has to be precise and undercutting small. It is almost impossible to satisfy all these demands at the same time. The Bosch process has been the dominant way to respond to these demands. Nowadays there is also another option that may be even more effective than the Bosch process. It is cryogenic reactive ion etching (RIE) that employs SF_6/O_2 -based high-density plasmas.

The principle of the Bosch process is shown in Figure 14. It is based on alternating etch and passivation steps. After lithography the Bosch process continues with a short etch step. The etching is done in sulphur hexafluoride (SF_6) plasma. After etch step a thin conformal fluorocarbon film is deposited on the silicon and photoresist. The fluorocarbon film passivates the surface and prevents etching. Octofluoro cyclobutane (C_4F_8) is commonly used in passivation step. At the beginning of the next short etch step the fluorocarbon film is removed from horizontal surfaces but sidewalls remain passivated. Even if SF_6 etch step is not fully anisotropic the polymer etches preferentially from the horizontal surfaces and vertical sidewalls remain protected. The repetition of etching and passivation steps results in almost vertical sidewalls and HARs and ERs can also be achieved [24]. The picture of the final structure etched with Bosch process is shown in the Figure 15. The sidewalls are vertical, but not very smooth. In many applications undulation on the sidewalls does not matter but Bosch process cannot be used if extremely smooth sidewalls are needed as in microoptics.

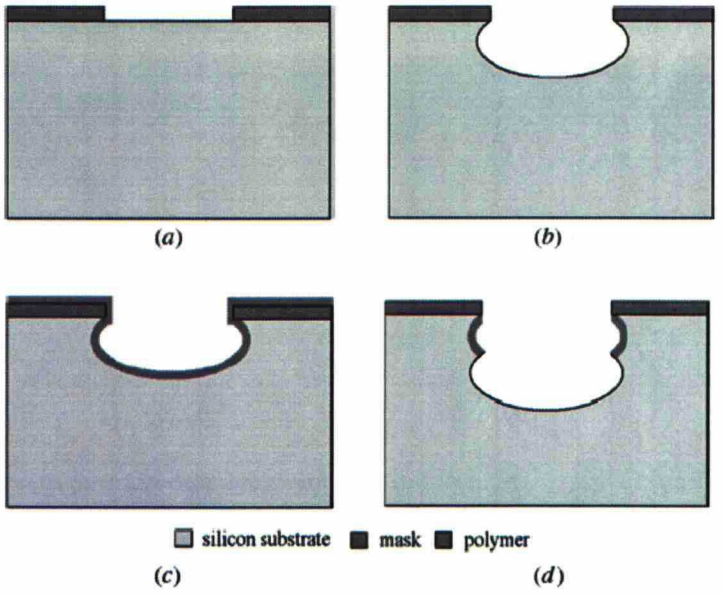


Figure 14. The Bosch process [25]. (a) Pattering. (b) Etching step. (c) Deposition of passivation layer. (d) Next etching step.

Figure 15. HAR pillars etched with Bosch process. The undulation resulting from repetition of the etching and passivation steps can be seen clearly [21].

3.1 History and development of cryogenic etching

Cryogenic RIE etching was first introduced by Tachi and his co-workers in 1988 [26]. The basic problem in plasma etching has been the inability to control separately etch rate of the bottom and the sidewall surfaces. This leads to isotropic etching profiles but the wanted etching result is almost always anisotropic. Different kinds of

trench profiles are presented in Figure 16. Another big problem is that it is hard to get good selectivity between silicon and masking material. Selectivity is defined with equation

$$selectivity = \frac{ER_{Si}}{ER_{mask}}, \qquad \{3\}$$

where ER_{Si} is the etch rate of silicon and ER_{mask} is the etch rate of masking material.

Tachi reported that by cooling the wafer during the plasma treatment the rate of chemical reactions on the sidewalls could be reduced dramatically and also the selectivity was improved [26].

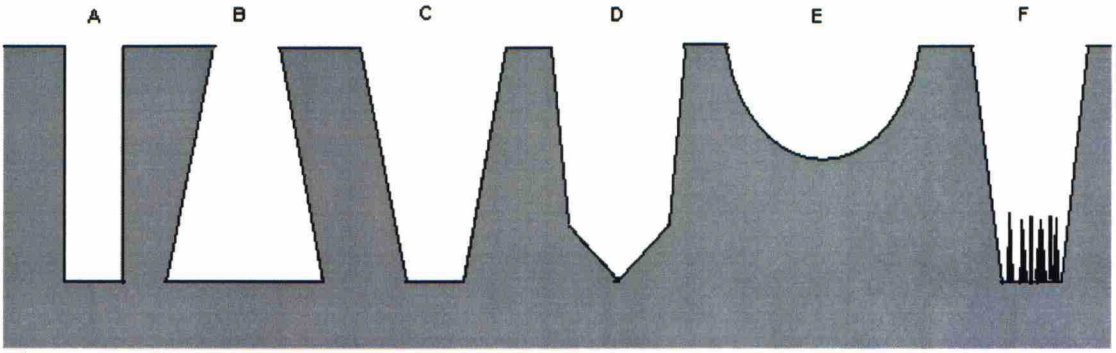


Figure 16. Different trench profiles. Trench A is a result of completely anisotropic plasma etching and it is almost always the goal of etch process. It has perfectly vertical sidewalls. Trench B has negatively tapered and trench C positively tapered sidewalls. Crystallographic dependent etching can be observed on the bottom of the taper D. Taper E is isotropically etched and black silicon appears at the bottom of the taper F. If black silicon is found, the sidewalls are usually positively tapered and etch rate is substantially lower than usually.

There are two main reactions in plasma etching. One is spontaneous chemical etching and the other is ion-assisted etching. Spontaneous etching takes place everywhere on the wafer, whereas ion-assisted etching takes place almost only on the horizontal surfaces because ions do not normally collide with sidewalls. Spontaneous chemical reactions lead to isotropical etching. The dependency between the rate of chemical reactions and temperature is presented in equation {4}. It is also know as Arhennius behaviour or Arrhennius rate law [27].

$$rate = z(T)e^{E_a/kT} \quad \{4\}$$

In equation above, E_a is the activation energy of the chemical reaction, k is Bolzman's constant, T is absolute temperature and $z(T)$ is a reaction dependent factor.

Tachi [26] concluded that at cryogenic temperatures anisotropy could be achieved because of the temperature dependency of spontaneous reactions. At low temperatures ER of the sidewalls should suppress substantially while ER of the bottom surface should decrease only slightly because ion-assisted reactions dominate in RIE [26]. After experiments Tachi and his co-workers noticed that anisotropy was good and ER of silicon was actually higher at the bottom surface when using temperatures below –100 °C. According to Tachi [26] ER was higher because of the low temperature increased the residence times of the atoms and physisorbed species on the wafer. Murakami and his co-workers obtained same kind of results a few years later [28]. In the early processes gas flows of the etchants were just a few sccm and whole cooling process was done with liquid nitrogen (see Figure 17).

Also Nakamura and Yano did RIE experiments at low temperatures in 1988 [29]. They used hydrogen bromide (HBr) as an etchant. They suspected that etching reaction products such as $SiBr_x$ attach to the sidewalls and protect them from lateral etching and mainly this residual layer protects sidewalls from etching. In 1995 Esashi and his group did low-temperature RIE experiments using SF_6 plasma [30]. Their main results were similar to earlier work but they suspected that lateral etching was reduced because of protective layer on the sidewalls even if they were using SF_6 as an etchant.

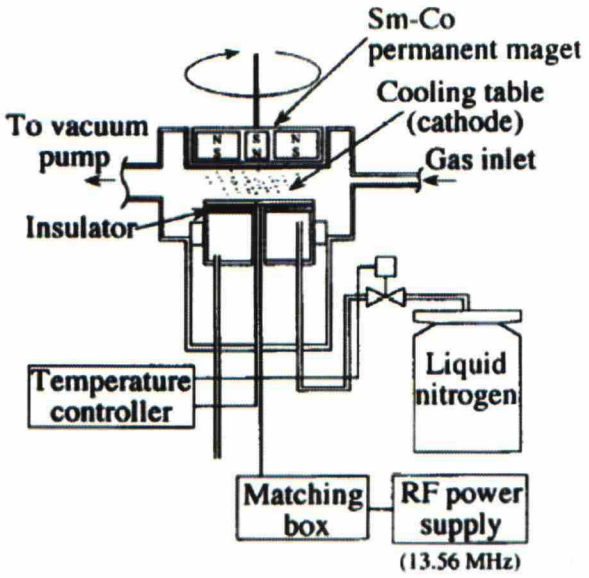


Figure 17. Schematic picture of the cryogenic RIE system that Murakami used [28]. Schematic picture of cryo-ICP RIE system used nowadays is shown in Figure 19.

In 1995 there were few publications where addition of oxygen (O_2) in SF_6 plasma was studied [31, 32]. These studies indicated that more than just low temperature was needed to get anisotropical etching result. In these new experiments the etching remained isotropical even though the temperature was low. The results at cryogenic temperatures were just slightly better than at higher temperatures and only when oxygen was added to plasma, good anisotropy could be achieved. They concluded that addition of oxygen caused the formation of passivation layer on the sidewalls because of the adsorption of oxygen atoms. The passivation layer is solid, inert and slowly etching material that stops lateral etching almost completely. Vertical ion bombardment removes the passivation layer from the horizontal surfaces and this is a mechanism that provides the anisotropic etching result (see Figure 18).

In the conditions where etching is completely vertical native oxide, particles, etc. will act as micromasks and silicon spikes will appear on the bottom of the etched surface. Too high oxygen content in SF_6 plasma can also initiate the spike formation. Because of the high oxygen content the silicon spikes have passivating silicon oxyfuoride coating. The heights of the spikes increase while etching proceeds. If spikes are taller than the wavelength of incoming light, the light will be trapped and cannot leave the

silicon surface anymore. Therefore the area turns black and it is called black silicon (BS) [31-34].

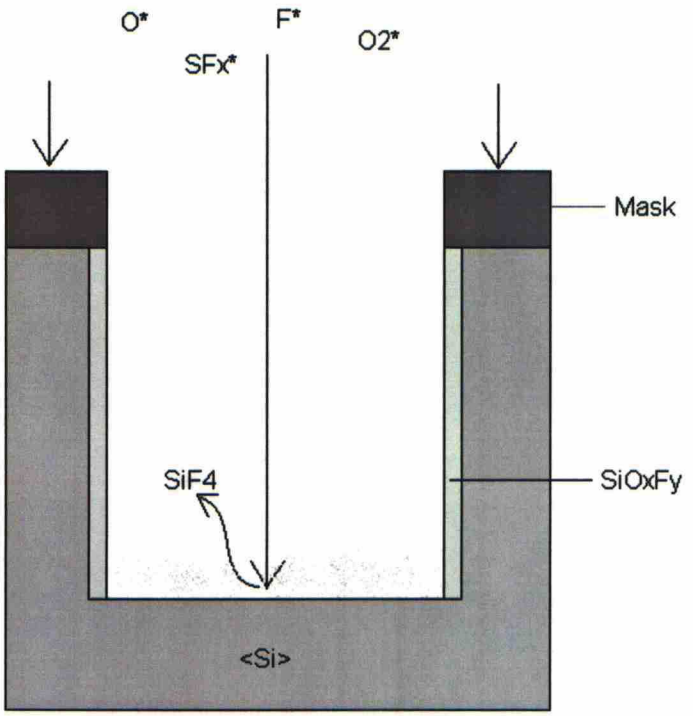


Figure 18. Sidewall passivation in cryo-DRIE process. A thin passivation layer on the sidewalls stops lateral etching. Directional ion bombardment removes passivation layer from the horizontal surfaces and etching proceeds.

Francou and his co-workers [31] studied the influence of substrate temperature on ER. They realized that ER of silicon got higher when temperature of the wafer was lowered even if the Arrhenius rate law suggests that the effect of lower temperature should be completely opposite (see equation {4}). Francou believed that increase in ER was because the condensation of the atomic fluorine increased when temperature was lowered. Higher fluorine condensation led to increased surface residence times of physisorbed reactive species. In physisorption the reactive species are absorbed by surface but there are no chemical bonds between the surface and physisorbed species. Therefore the binding energies are relatively small. At low temperature the amount of physisorbed reactive species increased and therefore the Si-F reaction rate increased and it resulted in higher ER of silicon [31]. Tachi made also same kind of assumption [26].

It has also been demonstrated that rate of ion-assisted etching is also temperature dependent [35, 36]. The reason to this is not well understood but at low temperatures ion bombardment enhances etch rate of silicon substantially at least in XeF_2 plasma.

Later also Jansen's group [37] discovered that ER is slightly higher at cryogenic temperatures than in room temperature. The study does not clarify why ER is higher, but it shows that if temperature is below –170 °C the condensation of SF_6 or S_xF_x species is too strong and the ER decreases rapidly. The condensation point of the SF_6 is approximately –194 °C [38].

Both Francou's [31] and Bartha's [32] groups also added helium cooling to the backside of the wafer to make sure that temperature of the wafer was same as the temperature of the liquid nitrogen cooled electrode. Still there is a difference between the temperature of the cooled electrode and the wafer [39]. Bartha [32] also concluded that inductively coupled plasma (ICP) source would be most suitable for cryogenic etching because in that kind of machine plasma density is higher than those obtained in capacitive discharges. Therefore plasma sheath thickness is substantially lower which ensure short ion paths and therefore the directionality of the ions is good and high bias voltages are unnecessary. This reduces surface damage and improves selectivity. Heavier ion bombardment in capacitively coupled plasma (CCP) source equipped machines also increases the substrate temperature [40].

After these publications nothing really new concerning etching in cryogenic temperatures was published for many years until cryo-etching equipment became commercially available in the beginning of the 21st century and many new articles were published [37, 39, 41-49]. Most of these articles concentrate on optimizing the etching process and parameters.

3.2 Influence of different parameters on the etching results

All new deep reactive ion etching (DRIE) machines that employ cryogenic temperatures have two RF-units that make possible to control separately ion density and ion energy (Figure 19). ICP plasma source creates high radical and ion concentrations and CCP source controls ion energies [37]. In these machines the temperature of the wafer can also be accurately controlled with helium backside

cooling. The wafer is mechanically or electrostatically clamped to cooled substrate electrode. The substrate electrode is cooled with liquid nitrogen and good heat transfer between the wafer and the electrode is ensured by helium flow on the backside of the wafer [41].

Usually vertical sidewalls, high etch rate and selectivity are desirable. The popular and fairly easy method to find etching conditions that result in vertical sidewalls is called "black silicon method". Too large oxygen content in plasma caused the formation of the BS. If vertical sidewalls and good anisotropy are needed the etching conditions have to be near the conditions where BS appears. Black silicon method is described in detail by Jansen [33]. In this chapter we concentrate on describing how changing one parameter should change the etching result.

It is quite difficult to change just one parameter at the time because usually the changes in one parameter also alter the other circumstances. E.g. higher helium backside pressure may also lead to higher helium leakage flow to process chamber and that can change plasma properties. Also wafer temperature is dependent on helium backside pressure. Some rough guidelines can however, be given.

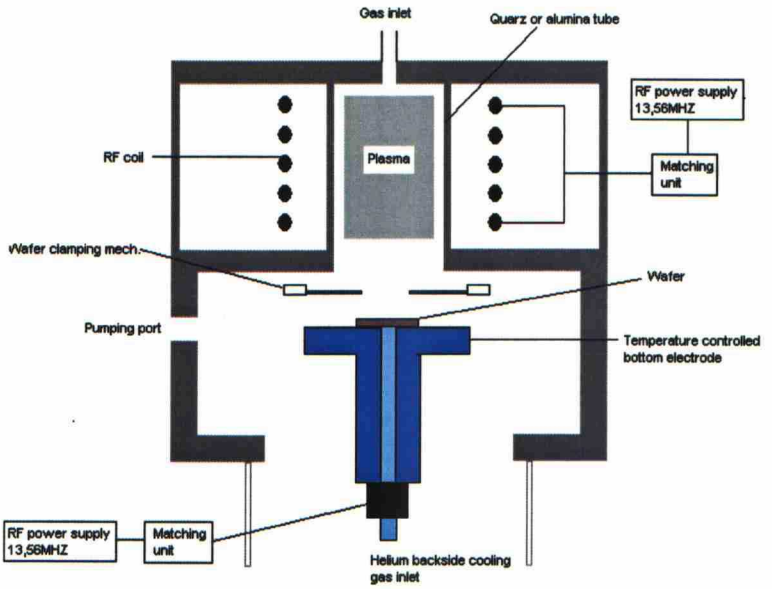


Figure 19. Schematic picture of the process chamber of ICP DRIE that employs cryogenic temperatures. The machine has two RF power units, nitrogen cooled bottom electrode, helium backside cooling system and mechanical wafer clamping system

Parameters that are usually changed when optimizing the process are the etching temperature, gas flows and powers of the plasma sources. The other parameters that have to be considered as well include process pressure of the chamber, helium backside pressure and clamping pressure of the wafer. It is also good to remember that etching results are also strongly influenced by other factors. E.g. change in the size or shape of mask opening, aspect ratio, loading or masking material may lead to completely different kind of etching result [50, 51].

3.2.1 Effect of temperature

When other parameters remain unchanged the angle of the sidewalls changes with temperature. At very low temperatures the sidewalls are negatively tapered. If temperature is raised, the angle of sidewalls changes slowly. At some point, depending on the other parameters, vertical sidewalls can be attained. If the temperature is raised too much, the sidewalls will become positively tapered at first and further temperature increase leads to isotropic profile. Therefore it is very important to be able to control the wafer temperature precisely. That is why the helium backside cooling is needed [37, 41]. It should also be taken into account that wafers always have some micro roughness and therefore only a small part of the wafer is actually attached to the cooled bottom electrode. It is also good to notice that at the cryogenic temperatures thermal conductivity of heavily doped silicon is ten times poorer than thermal conductivity of undoped silicon [52].

Etch rate remains almost constant above 100 K if black silicon is not found. ER decreases rapidly if BS is formed or the temperature cools below 100K. At lower temperatures the condensation of SF_6 is too strong and etching cannot proceed. Otherwise the ER slowly decreases if temperature is increased [37, 41].

Crystallographic dependent etching can also be observed when lowering the temperature enough. Like in anisotropic wet etching the (111) planes of silicon are etched slower than (100) and (110) planes. This effect can only be seen at very low temperatures and with low ion energies. Raising the process pressure can enhance this effect. At higher temperatures this effect cannot be seen because fluorine has higher reactivity and its reaction products are more volatile [41, 43]. If etching

products are not volatile they may form a solid film on the surface of the silicon and it may act like a passivation layer.

3.2.2 Effect of oxygen

Oxygen content is the most important parameter when adjusting the angle of sidewalls. If there is no oxygen present in the process chamber the etching result is isotropic as mentioned before [31, 32]. If oxygen content is too low the sidewalls are negatively tapered and bottling is also usually observed. The reason to bottling is the local removal of thin passivation layer on the sidewall by the impact of the ions. If process pressure is high, bottling is pronounced due to dispersion of ions. The higher regions of the sidewalls are bombarded and etched by off-normal ions (see Figure 38). Negatively tapered sidewalls are due mirror charge effect or back scattered ions that reflect from the bottom of the trench. When oxygen content is raised the quality of the inhibitor layer silicon oxyfluoride (SiO_xF_y) is improved and vertical sidewalls are achieved. If oxygen content is too high it leads to overpassivation and initiates the formation of black silicon and sidewall angles will become positive [40, 41].

3.2.3 Effect of SF_6 flow, ICP and CCP powers

Increasing the ICP power has same kind of effect as higher SF_6 flow because both parameters influence the concentration of the fluorine species. Increase in one or the other parameter also increases the etch rate of both silicon and passivation layer and etching profile changes to more negatively tapered. Too low ICP power or SF_6 flow leads to positive sidewall profiles and formation of black silicon [41].

CCP power controls ion energies. The removal rate of the passivation layer is related to ion energies. Too high CCP power results in too thin passivation layer, negative sidewall profiles and bottling, whereas too low CCP power may initiate the formation of black silicon and cause positive sidewall profiles [41]. CCP power also affects selectivity very strongly. Erosion of the mask increases almost linearly with CCP power because ion velocity and energy increase with CCP power. High-energy ions may be able to break the bonds of the masking material and erode its surface by forming volatile compounds. Etch rate of silicon is usually not linearly dependent on

CCP power and therefore selectivity is usually lower when CCP power is increased [37].

3.2.4 Effect of process pressure

Process pressure is also an important parameter, but sometimes it cannot be controlled independently. If gas flows are too high the vacuum pumps cannot maintain low pressure. Efficiency of the vacuum pumps is the factor that determines the maximum gas flows. The maximum process pressure is normally considered to be 10 mTorr [41, 42]. If higher pressures are used, the mean free path of the ions becomes too small and ions experience collisions before hitting the surface of the wafer. Because of the collisions the ion bombardment is not directional and bottling appears as discussed above. High process pressures may also cause crystallographic dependent etching [41, 44]. Additionally Boufnichel and his co-workers measured that mask undercutting increases almost linearly with process pressure [44].

3.2.5 Helium backside cooling

Backside helium pressure of the wafer is also one parameter that must be fixed before etching. The function of helium pressure is to control the heat exchange between the wafer and cooled electrode. Clamping pressure controls the sealing of helium backside chamber. If this clamping pressure is too low or helium pressure is too high helium leaks into chamber and heat exchange between the wafer and the electrode is compromised. This reduced heat exchange causes a higher than expected wafer temperature and this changes the etching profile decidedly as discussed above [41].

The pressure difference between the two sides of the wafer induces wafer mechanical deformations (see Figure 20). Due to these deformations the contact area of the wafer and the electrode gets smaller and temperature differences within the wafer gets more pronounced. Because the wafer is clamped from its edge, the edge of the wafer is cooler than the centre [39].

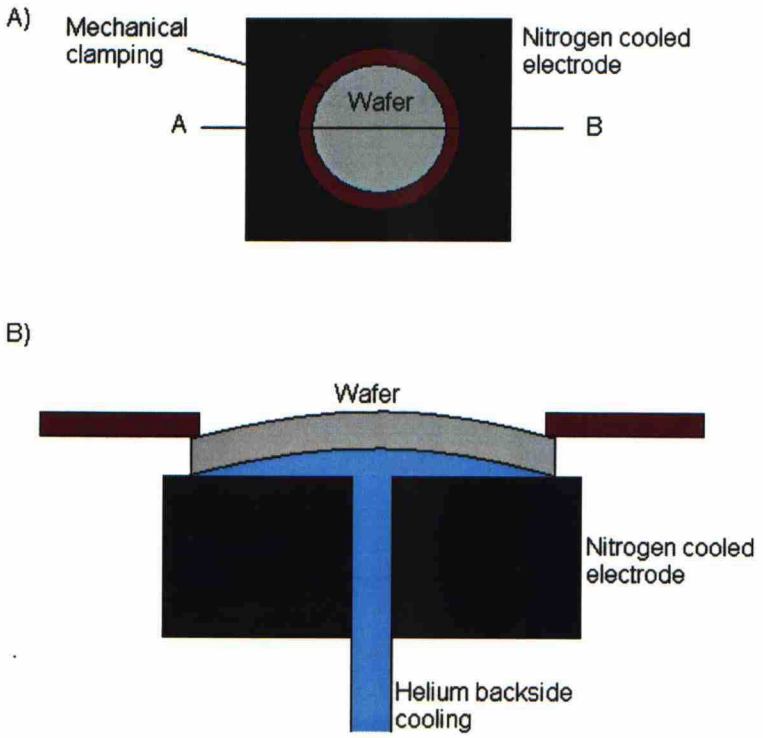


Figure 20. Wafer deformation induced by helium backside pressure. (A) Top view. (B) A cross-section of line AB.

3.2.6 Conclusions

All the parameters mentioned have some effect on the result of the etching. These are graphically presented in Figure 21. Usually temperature, helium and clamping pressures are fixed and the main adjustable parameter is the oxygen flow. It is important to notice that when etching time is changed the recipe may require some kind of finetuning because aspect ratios change as well. Also different sized mask openings need different kind of recipes if anisotropic etching profile is required [41, 42].

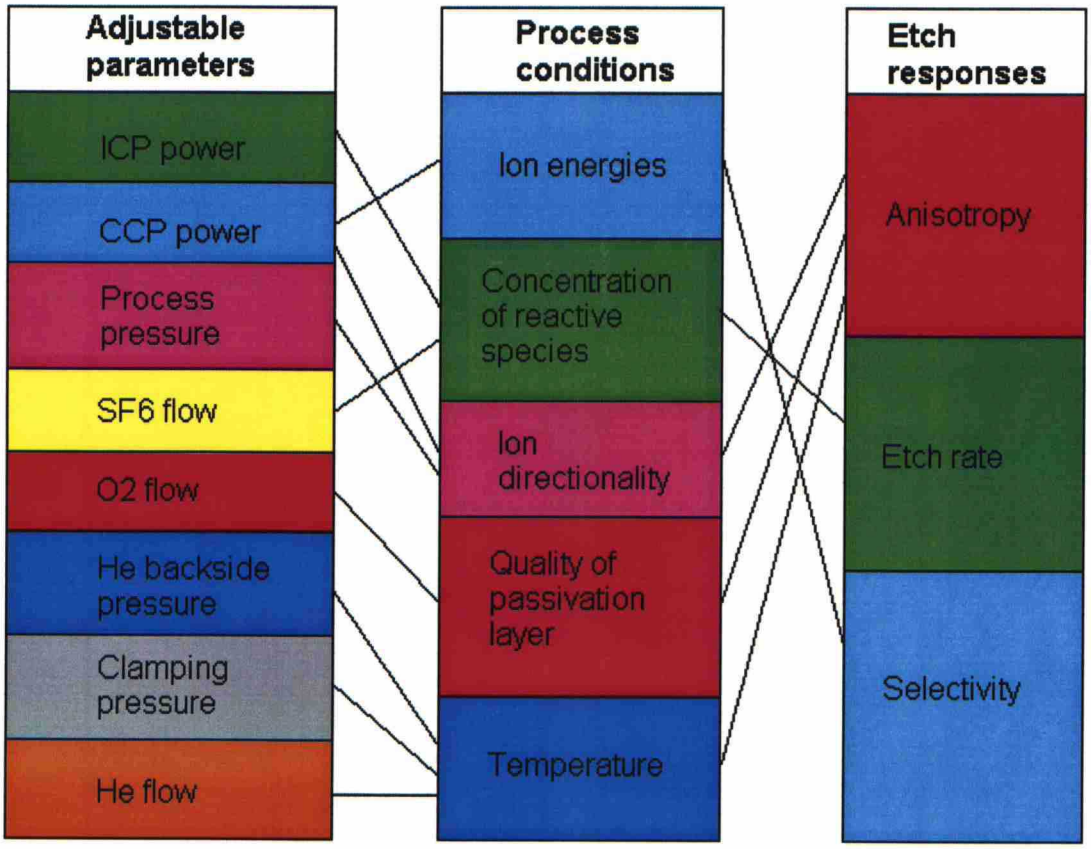


Figure 21. The effect of adjustable paramters on process conditions and etch responses. Diagram that shows how process conditions change if one parameter is changed and how that affects to final result. The picture is very simplified. Attention: the main thing that decides wafer temperature is the temperature of the liquid nitrogen cooled bottom electrode. Helium just makes thermal conductivity better.

3.3 Passivation mechanism in cryogenic SF_6/O_2 etching process

There have been a lots of speculation on reasons why cryo-etching is anisotropical. At first, it was suspected that anisotropical etching was achieved because of the reactions of the free radicals were reduced so much because of the lower temperature [26]. Then it was noticed by many groups that there were also some kind of passivation layer on the sidewalls that protected trenches from lateral etching [31, 32, 45, 46]. It was found that oxygen content of plasma seemed to have crucial effect to the quality of this passivation layer. For long it has been unclear how this layer is formed and removed because there are no residual layers on the silicon surface after the process.

In 2004 a study that seems to have solved this question was published [45]. According to Dussart and his co-workers, the reason why SiO_xF_y layer worked as a passivation layer was fluorine's low adsorption coefficient to this SiO_xF_y layer. They also concluded that passivation layer could form only at cryogenic temperatures and if the temperature of the wafer was raised, the passivation layer vanished almost completely. Sulfur played no role in formation of this layer. Oxygen mostly defines the quality of the passivation layer but fluorine is also essential in formation process [45].

A year later an article on formation of SiO_xF_y passivation layer was published [46]. Mellhaoui et al. believe that silicon oxyfluoride layer is created in reaction between SiF_x species deposited on the sidewall and oxygen radicals. In SF_6/O_2 plasma SF_6 etches silicon and common reaction product is SiF_4 that creates SiF_x species in the plasma. SiF_x species deposit on the silicon surface because their sticking coefficient on silicon is close to 1. When oxygen radicals react with deposited SiF_x molecules the SiO_xF_y layer is formed. Another possible scenario is that fluorine atoms provided by SF_6 diffuse on a silicon surface and form SiF_x species without volatile intermediate SiF_4 product [46].

4 Etch rate and selectivity experiments

The purpose of these experiments was to measure the etch rate (ER) of silicon and the selectivity of the photoresist (PR) against silicon in Oxford Instruments Plasmalab System 100 - ICP 180 equipment. Three wafers and three different etching times were tried.

Ideally the etch rate and the selectivity should be constants but in reality e.g. the aspect ratio of the etched structure, loading and size and shape of the mask opening play also an important role in etch rate (see Figure 22). It is important to notice that selectivity is ratio. If etch rate of silicon changes the selectivity alters also even if the ER of mask would not be affected [24].

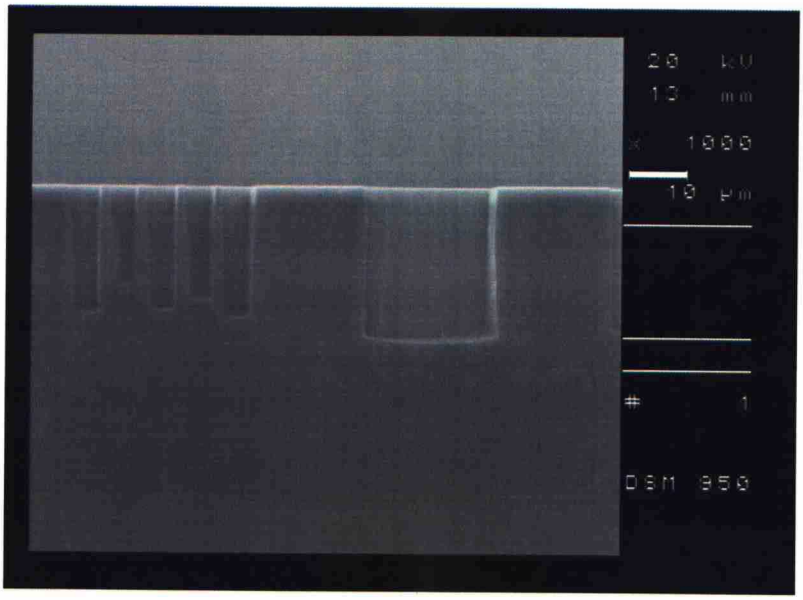


Figure 22. Etching depth is affeced by the size of the mask opening. This phenomenon is termed RIE lag.

4.1 Wafers

Double side polished (DSP) 100 mm wafers were used and their thickness was 381 µm ± 15 µm. Their crystal orientation was <100> and they had p-type doping. The resistivity of the wafers was 6,1 - 8,4 Ωcm. Standard RCA1, RCA2 and HF cleanings had been done according to Figure 23 to the wafers when they were taken into the clean room.

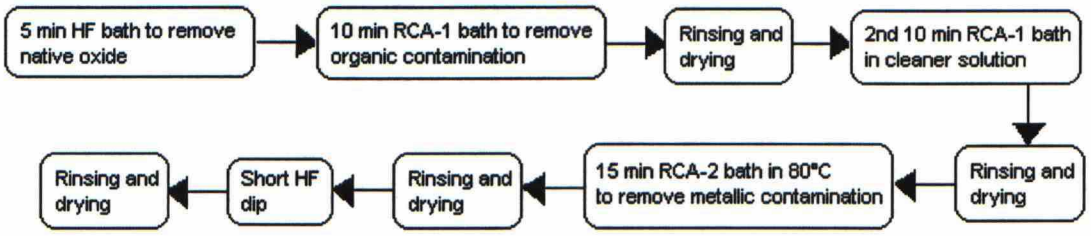


Figure 23. Flow chart of wafer cleaning steps. All the wafers that are brought into the clean room are washed carefully. This ensures that the wafers are clean before processing starts. Dirty wafers could aslo contaminate the processing equipment.

After cleaning, the wafers were stored on the shelf of the clean room for 2 months. Therefore a thin native oxide film was on the wafers and also some organic contamination from the wafer box when processing started.

4.2 Lithography

The lithography was done to the wafers according to flow chart in Figure 24. AZ5214 photoresist was used and exposure was done with Electronic Visions AL6-2 mask aligner. The exposure time was 4 seconds. Loading of the etch test mask was 50%. The post bake of the first wafer was only 30 minutes.

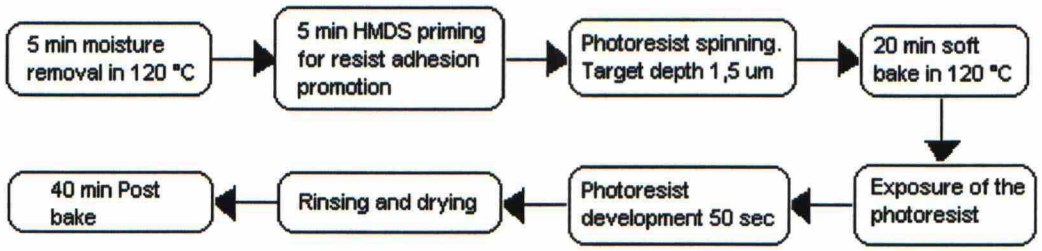


Figure 24. Flow chart of used lithography step.

4.3 Test structures

The patterns on the mask are presented in the Figure 25. Most of the test structures are lines and squares, but there are also test structures that are designed to resistivity measurements and mask aligning. The most of the experiments are done with this etch test mask.

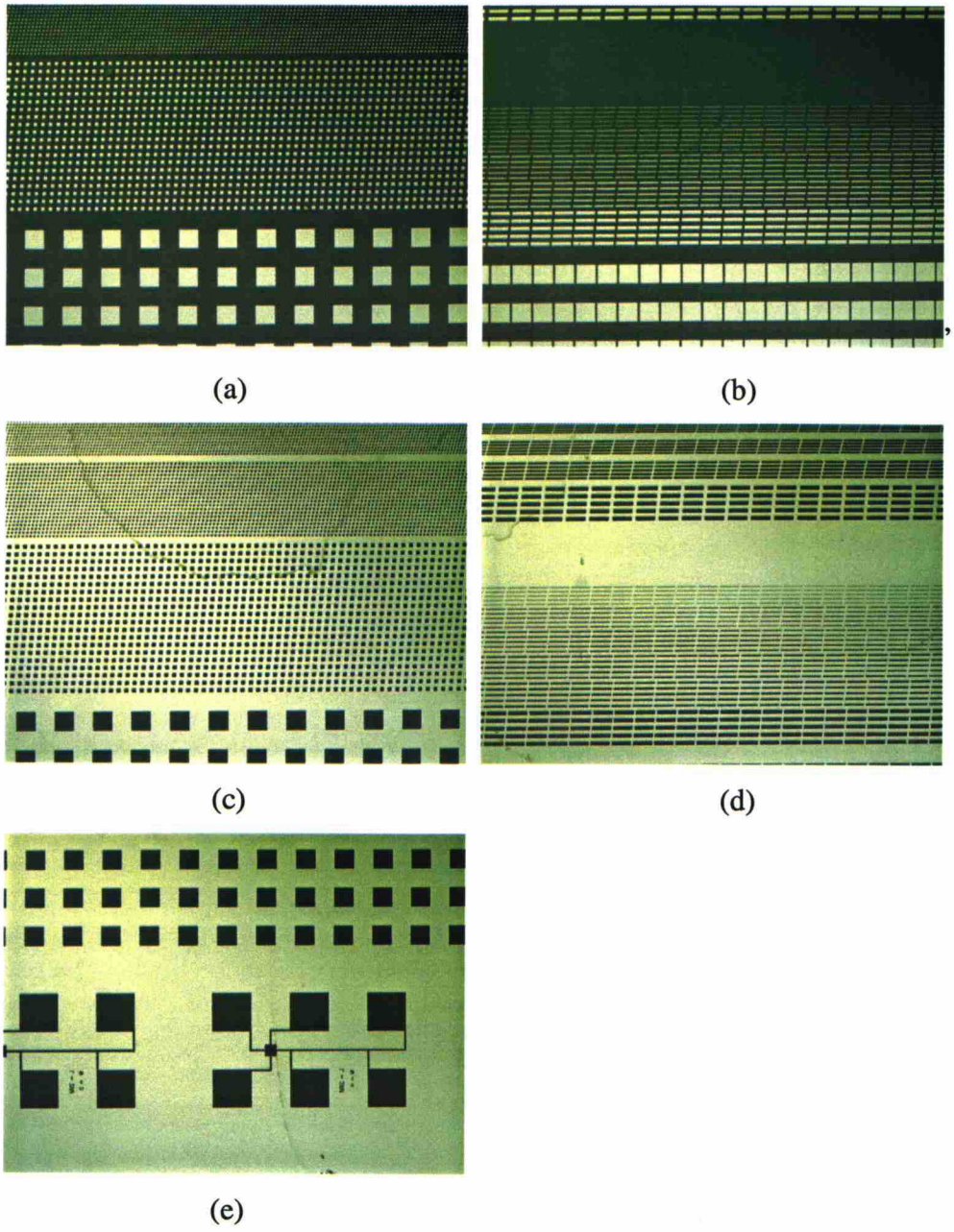


Figure 25. The patterns of the test maks. The mask has two different chip types. Pictures (a) and (b) are from the chip that results in holes. The dimensions of the largest square are 20 μm x 20 μm. The smallest line width of the line is 1 μm. Pictures (c) - (e) are from the second chip. The chip is negative image of the first chip. Therefore the dimensions of the patterns are the same, but chip produces pillars. The etchable area of the second chip is considerably larger. There are also a few other test strcutures on the chips, e.g. electrical line width stucture shwn in (e).

4.4 Etching

The temperature range of the DRIE equipment is from –150 °C to 400 °C. The power supply unit of ICP power is 2 kW and the power supply unit of the CCP power is 300 W. Mass flow controllers limit the maximum flow rates of gases to 100 sccm / line.

The first etching process was done with dummy wafer at room temperature. The purpose of this process was to clean the chamber because the previous sample etched was InP and there were probably some residues in the chamber. After the cleaning etch, the temperature of the substrate electrode was set to –110 °C. Cooling of the electrode took approximately 15 minutes. Wafer was then inserted into the reaction chamber for 3 minutes. Backside pressure of the helium was 10 Torr. The purpose of this step is to cool the wafer down to –110 °C.

Parameters of baseline etch process are shown in the Table 1. All three wafers were etched under these conditions, but backside pressure of helium was only 3 Torr because of minor problem of the clamp mechanism. Helium flow to process chamber would have been too high if 5 Torr backside pressure was used.

Table 1. Process parameters of the baseline etch process. Plasma is struck in the 15 mTorr pressure.

Etching time	Process pressure	SF_6 flow	O_2 flow	Temperature	He pressure / flow	ICP power	CCP power
Varies	10 mTorr	40 sccm	6 sccm	-110 °C	5 Torr / 10 sccm	500 W	3W

4.5 Experimental results

Etched wafers were inspected with an optical microscope. Some cracks in the photoresist of the first wafer could be seen. The cracks were quite large and they could be seen also without a microscope. PR cracking will be discussed in more detail in chapter 6.

The combined depth of etching and remaining resist was measured with a profilometer. Two measurements were taken from the edge of the wafer and one from the centre. Average thickness was calculated. Resist was removed according to flow chart of the Figure 26 and optical microscope inspection was made to ensure

that resist was removed completely. The profilometer measurements were repeated and the etched depth of silicon was obtained.

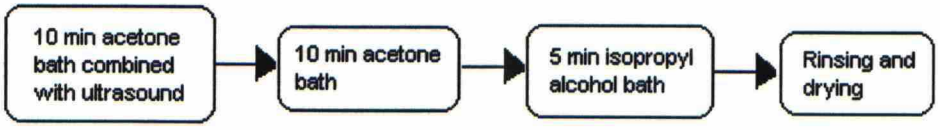


Figure 26. Flow chart of photoresist removal step.

It can be concluded from Figure 27 that the etching of silicon did not start immediately when process was started. This is because of a thin native oxide film and organic contamination on the silicon wafer. Ca. 15 seconds was the time needed to remove the native oxide and organic contamination that had grown on the wafers. Etch rate can be calculated from the trendline of the Figure 27. It is the slope of the line. In this experiment the etch rate was ca.1,7 μm/min.

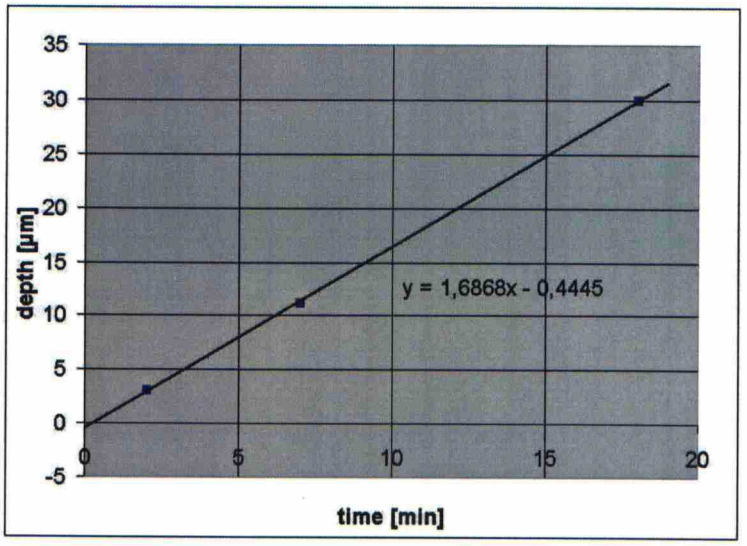


Figure 27. Measured etch depth in function of time. Linear trendline is drawn according to results. Etch rate is ca. 1,7 μm/min. Etching of silicon does not start immediately when process starts because there was a thin residual layer on the wafer. This is also the reason why trendline does not go through the origo.

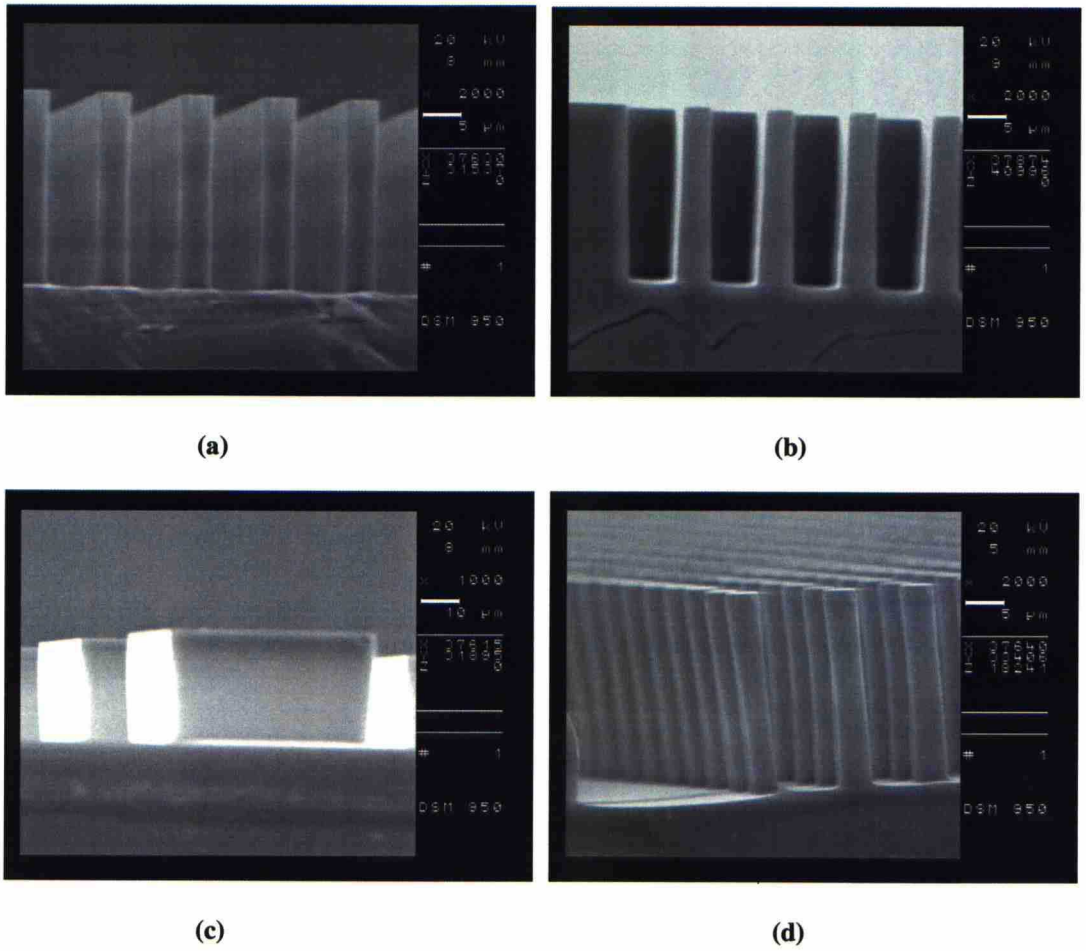
The results of the profilometer measurements and calculated PR erosion values are presented in Table 2. It is good to notice that PR erosion of the two last wafers is exactly the same. This cannot be true. The problem is the inaccuracy of the

profilometer. The trenches that were etched 18 minutes are so deep that only a small percentual error is enough to corrupt the PR erosion calculations.

Table 2. Results of the profilometer measurements and calculated etch PR erosion during the process.

Wafer number	Etching time	Measured PR thickness before etch	Measured remaining PR + etch depth	Measured etch depth without PR	Calculated PR erosion
1.	2 min	1,45 μm	4,52 μm	3,11 μm	0,04 μm
2.	7 min	1,45 μm	12,2 μm	11,1 μm	0,35 μm
3.	18 min	1,55 μm	31,2 μm	30,0 μm	0,35 μm

In Figure 28 there are four scanning electron microscope (SEM) pictures. It can be seen that some of the pillars are vertical and smooth but walls of the grooves are not perfect. Barrelling can be seen. The shape of the large pillar is far from perfect. As discussed in the chapter 3.2.6, different sized structures cannot all be perfect if etching is done in one process. In other words, the mask opening and etching profile have a connection as reported [41, 51]. This is the reason why it is important to use approximately same line widths in the same mask and the etching process should be optimized to this particular line width.



(a) (b)

(c) (d)

Figure 28. SEM pillars of silicon pillars. (a) Pillars that have vertical smooth sidewalls. (b) Some barreling can be seen in the grooves. (c) Large pillars are not perfect even if smaller structures on the same wafer had vertical sidewalls. (d) The small pillars have very smooth surface and the anisotropy is good. Pictures (a), (b) and (c) are from the same wafer and the process conditions were as in Table 1.

Figure 29 shows that the ER is increasing slowly because the wafers were not completely clean before processing started. Therefore native oxide and other residual materials on the wafer had to be etched away before silicon etching could start. According to literature the ER of the oxide is substantially lower than ER of the silicon [41].

The more common trend is that etch rate actually decreases during the DRIE process. This is because the aspect ratio gets higher as etching proceeds and higher aspect ratios result in depletion of etching species. This phenomenon is called aspect ratio dependent etching (ARDE) [24].

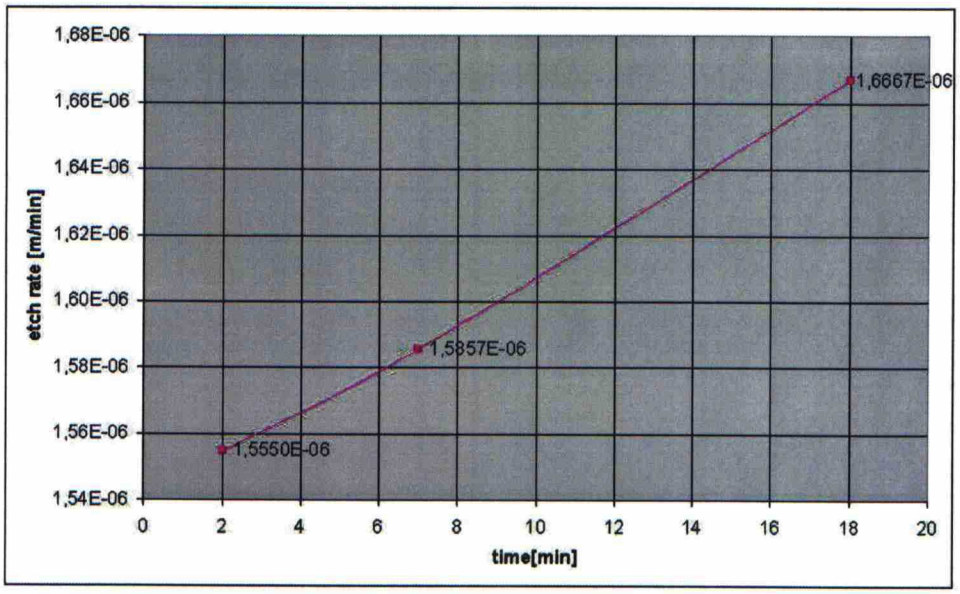


Figure 29. Silicon etch rate as a function of time. The ER increases while etching proceeds because there were a native oxide film and organic contamination on the wafer before etching started.

Estimate of PR selectivity against silicon can be calculated with equation {3} and it is approximately 50. Because resist degeneration calculations were not definite, exact value to selectivity cannot be calculated. Publications put the selectivity between photoresist and silicon to higher than 500 [41]. This selectivity was attained when loading was only less than 10%. The other parameters may also affect to selectivity, especially CCP power [37, 41].

5 Loading effect experiment

Etch rate of silicon is dependent on etchable area. This phenomenon is the called loading effect. The effect on ER can be observed in three different scales.

1. In batch reactors the etch rate is dependent on the number of the wafers that are etched simultaneously.
2. In single wafer reactors the ER degreases when etchable area of the wafer is raised.
3. The third scale of loading is called microloading and it means that the local etch rate depends on local feature density. In other words, the ER of the chip that has small etchable area is higher than the ER of the chip that has large area to be etched. Because of microloading effect dense array of lines etches slower than isolated lines. The depths of the outermost lines of the arrays are deeper than the others.

The profiles of the etched structures may also differ if loading is changed. This phenomenon called profile loading could not detected in the experiments presented in this chapter. All the loading effects are because of depletion of the etchant species. This may also create etch depth non-uniformity. Loading effect is strong when chemical etching is the main etching mechanism and etch rate is high [24, 50].

5.1 Experiment

To define the degree of loading effect in our single wafer reactor, three wafers were etched. Same mask was used as in the previous experiment but now an extra mask that covered some of the test chips was placed on the glass mask. In this way the loading could be changed from wafer to wafer. Etching parameters remained unchanged. The differences in etching depth, structure profiles and the etch rate of photoresist were observed.

Another concern was to define the radial uniformity in our equipment. Etch depth at the middle of the wafer was compared with the etch depth at the edge of the wafer. Radial uniformity was defined from the same wafers as loading effect.

The microloading measurements were done with the wafers etched in the previous experiment. Like shown in the chapter 4.3 there are two different types of chips on the wafers. One has different sized pillars on it and the other is the negative of the first chip. The loading of the pillar chip is approximately 75 %. The other chip that has trenches on it has 25 % loading. By comparing the local etch depths and rates of these two chips, the degree of microloading effect in our reactor was determined.

The lithography step that was used to pattern the wafers was similar to lithography step shown in the Figure 24. However, the exposure tool was different and standard exposure time had to be doubled because of the extra mask. Still, the smallest line widths were not exposed properly because the extra mask disturbed the propagation of light. In this experiment that did not matter, because the exposed wafer area did not change remarkably.

Baseline etch process was utilized (see Table 1) to etch all three wafers. Etching time of the wafers was 7 minutes. Optical microscope inspection was made after etching. The same observation could be made as before. The AZ5214 resist of the first wafer had cracks in it. The PR of the second wafer was intact but the PR of the third wafer was also slightly damaged after the etching process. Despite of cracking, the loading of the wafers remained almost unchanged.

5.2 Experimental results

5.2.1 Loading effect and radial uniformity

To determine the etch rate and radial uniformity of etching, profilometer measurements were performed after processing and the results are shown in the Table 3 and in the Figure 30.

It can be seen that loading effect was very strong. On the wafer whose loading was 50% the etch depth was only 62 % of the etch depth of the wafer that had 2 % loading. This means that loading effect has to be considered when designing a new process.

Table 3. Etch depth measuremets of the loading experiment. Measurements were repeated three times and average depths were calculated. Resist thickness was measured only once. Data for 50 % loading information was obtained from previous experiment (Table 2).

Loading	2 %	11 %	32 %	50 %
Resist thickness	1,50 μm	1,48 μm	1,48 μm	1,45 μm
Resist thickness + etch depth	19,1 μm	16,7 μm	13,7 μm	12,2 μm
Etch depth at centre	17,9 μm	15,6 μm	12,3 μm	11,1 μm
Etch depth at edge	17,7 μm	15,1 μm	12,4 μm	11,5 μm

Radial uniformity of etching can also be obtained from etch depth measurements (see Figure 30). There are two lines in the graph. The other one is from the measurements that were taken from the middle of the wafer and the other one is obtained form the measurements that were taken from the edges of the wafer. The standard definition for uniformity is

$$U = \frac{\max - \min}{\max + \min} * 100\%. \qquad \{5\}$$

Radial uniformity of our reactor is presented in the Table 4. It is very good. 5 % is considered as a typical performance to etch process [27].

Table 4. Radial uniformity of etching. The numerical values are from the loading experiment and the uniformity is calculated with equation {5}. Baseline process was used and the parameters are presented in Table 1.

Loading	Max	Min	Uniformity
2 %	18 μm	17,5 μm	1,4 %
11 %	15,7 μm	14,7 μm	3,3 %
32 %	12,5 μm	12,3 μm	0,8 %
50 %	11,7 μm	11,1 μm	2,6 %

In this experiment the etch rate was higher at the centre of the wafer when the loading was small. When loading was greater than 30 % the etch rate was higher at the edges of the wafer. This kind of behaviour is detected also elsewhere and it is

because the fluorine depletion is greater at the centre of the wafer because of reactor geometry [24, 53]. High pattern density usually results in higher etch depth variations [53]. By increasing the SF_6 flow, the etch depth variations could be reduced [54].

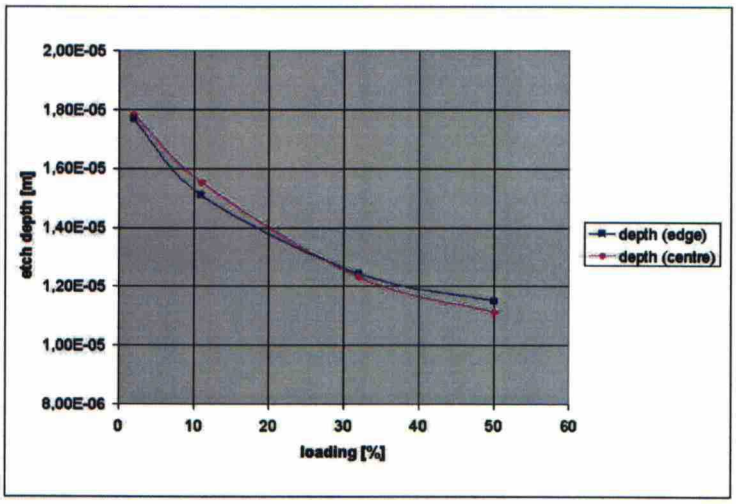


Figure 30. Etch depth in function of loading. Etch time was 7 minutes. Loading effect is strong in our reactor. The uniformity of the etching is good.

In this experiment, the connection between loading and ER of the photoresist could not be found. Measured photoresist erosion varied from 10 nm to 40 nm. There is no real point in calculating selectivity of the PR against silicon because exact etch rate of PR remains unknown. Some kind of rough estimate can still be calculated with the equation {4}. Usually ER of etching mask material is not loading dependent. Therefore selectivity increases when loading is decreased [55]. Highest selectivity is obtained with smallest loading because etch rate of silicon is then at its maximum. When loading is 2 %, the selectivity is almost 70.

5.2.2 Microloading

Profilometer measurements were performed to two wafers which both had 50 % loading. The etching time of the first wafer was 7 minutes and the etching time of the second wafer was 2 minutes. Three trenches (chip loading 25 %) and three pillars (chip loading 75 %) were measured from the centre and from the edge of the each wafer. The results are shown in Table 5.

There is a clear difference in structure heights between these two different chips. As suspected, the heights of the pillars were smaller than depths of the trenches because there was more area to be etched on the pillar chips. This led to local depletion of the etching species and resulted in different structure heights. It seems that effect of microloading gets relatively smaller as the process proceeds. Microloading effect is as strong on the edge of the wafer as at the centre of the wafer.

Table 5. Microloading measurements. The loading of pillari chip is approximately 75 % and the loading of trech chip is approximately 25 %. Height difference at the centre of the wafer is 6 % when etching time is 2 minutes and 4% when etching time was 7 minutes. At the edge of the wafer height difference is 7 % when etching time is 2 minutes and 4 % when etching time is 7 minutes.

Etch time	2 min	7 min
Trench depth at centre	3,12 μm	11,1 μm
Pillar depth at centre	3,01 μm	10,6 μm
Trench depth at edge	3,18 μm	11,5 μm
Pillar depth at edge	2,97 μm	11,0 μm

In array features the microloading effect could not be seen. All the trenches of the Figure 31 have equal depths.

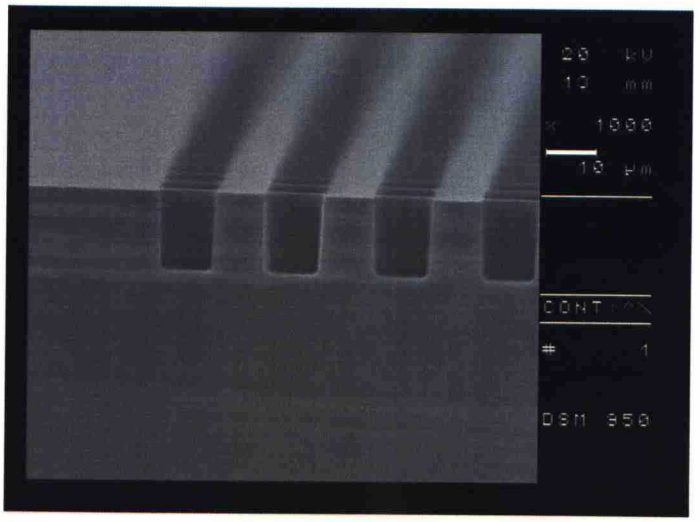
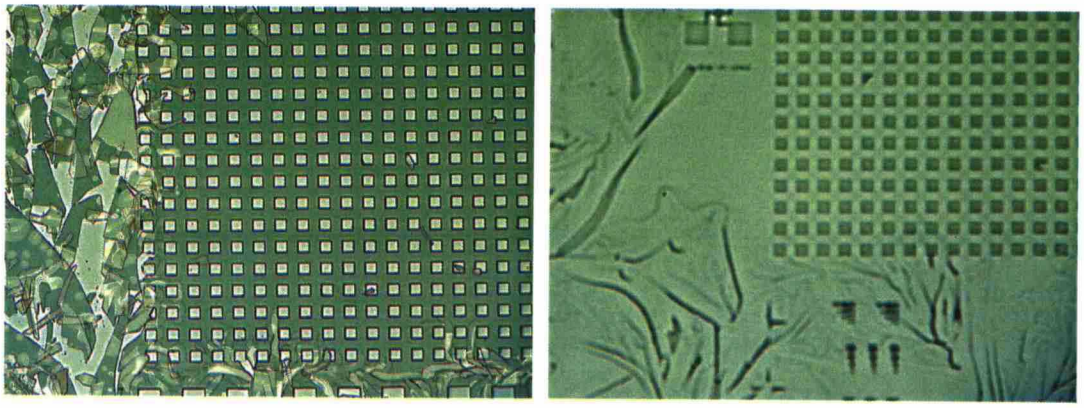


Figure 31. No microloading can be seen. All of the trenches are equally deep.

6 Photoresist cracking at cryogenic temperatures

As discussed before there have been problems with the stability of the PR at cryogenic temperatures. Sometimes during etching process photoresists have shattered like glass (see Figure 32a). Most of the cracks have been on the edges of the wafer but sometimes the whole resist has been badly damaged. Large solid resist areas are more prone to cracking than small areas. It is also clear that photoresist cracking is not just aesthetic flaw, but it also affects strongly etching results (see Figure 32b).



(a) (b)

Figure 32. (a) Photoresist cracking after etching. Especially large continuos resist areas are almost completely destroyed. (b) The effect of PR cracking to the final result. PR cracking is fatal error.

This phenomenon has not been the focus of any scientific article. It is known that over 1,5 μm thick photoresist has tendency to crack when cooling the resist to cryogenic temperatures [42]. It is distracting that sometimes these cracking problems arise and sometimes photoresist behaves very well also at the low temperatures. Silicon dioxide, silicon nitride and aluminium masks were also used at cryogenic temperatures but they did not show any problems.

6.1 Experimental results

6.1.1 Reason to photoresist cracking

To get some sense to PR cracking phenomenon few experiments were carried out using AZ5214 resist. First, the effect of the post bake duration was studied. Post bake

times from 20 to 60 minutes were tested but no relation between the cracking and the post bake duration could be found.

The manufacturer of the PR recommends that etching should be done immediately after post bake or post bake should be repeated before etching if lithography is done long before etching. Therefore it was tested if rebaking just before etching could inhibit PR cracking. Again, random behaviour of the resist was detected. Some many months old photoresist layers did not have any problems at cryogenic temperatures while some fresh resists cracked.

After this it was sorted out in which part of the process the photoresist cracks. Therefore the wafer was loaded inside the cooled process chamber, kept there for a minute and taken out. It was found out that photoresist does not crack before process starts. Then the wafer was loaded back in the chamber and only three minutes long wafer cooling was carried out. The backside pressure of helium was 10 Torr. It was discovered that after cooling period the photoresist was already damaged and therefore it was concluded that backside helium pressure plays a role in cracking phenomenon. High backside helium pressure is used during the cooling period before the etching and that creates wafer deformation [39] that may initiate PR cracking (see Figure 20).

One minute cooling period before turning the helium backside pressure on was found out to reduce the cracking probability but still the problem did not disappear completely. Also lower helium backside pressure during the wafer cooling may also help.

6.1.2 Behaviour of different photoresist materials

The behaviour of three different resist types was tested at cryogenic temperatures and the results are presented in the Table 6. The behaviour of AZ5214 was discussed already in previous section. AZ4652 resist cannot be used at cryogenic temperatures because 3 μm thick resist was completely covered with cracks after cryo-DRIE process. Surprising result was that even 70 μm thick SU-8 layer did not experience any cracking problems. Three different resist thicknesses were tested and all of them were flawless after processing.

Table 6. Cracking of different photoresists. Etching conditions: ICP power 1000 W, CCP power 3 W, temperature –110 °C, etching time 7 minutes, thermailization period 3 minutes, maximum backside helium pressure 10 Torr. Loading 50 %.

Photoresist type	PR thicknesses	Cracking problems
AZ5214	1,5 μm	Some
AZ4562	3,0 μm	Yes
SU-8	7,0; 20; 70 μm	No

7 Oxide mask

If high selectivity is needed SiO_2 mask is often used in DRIE process. The selectivity of the thermal oxide mask against silicon is reported to be somewhere around 1000:1 at cryogenic temperatures [41, 42]. In some articles even selectivity of 10000:1 is achieved under optimal process conditions [37].

7.1 Wafer cleaning and oxidation

When new wafers are brought into the clean room they have to be cleaned before processing. It is especially important to clean the wafers properly before thermal oxidation because in furnace processes contamination diffuses deep into the wafer. Standard cleanings were done before oxidation according to Figure 23. Then, the wafers were wet oxidized for 50 minutes in 1050 °C. Created oxide thickness was 422 nm.

7.2 Experiment

The first experiment was carried out with one wafer. The oxide layer on the wafer was patterned with photoresist. The test mask presented in chapter 4.3 was used. Same lithography step was used as before (see Figure 24). The etching of the oxide was performed in buffered hydrogen fluoride (BHF) solution. Then PR was removed using the procedure outlined in Figure 26. The baseline etch recipe presented in Table 1 was used, but the helium flow to chamber was only 5 - 6 sccm. Etching time was 18 minutes.

7.3 Experimental results

7.3.1 Etch depth measurements

The etch results were completely different from the experiments discussed in chapters 4 and 5. After DRIE etching of silicon, there could be seen without a microscope that oxide layer had been etched away from wafer centre. All of the areas that were clear form oxide before etching had turned to black.

The thickness of the remaining oxide layer was measured with ellipsometer. In the middle of the wafer the remaining oxide layer thickness was under 100 nm whereas on the edge of the wafer the thickness of the oxide layer was over 300 nm. The

uniformity of the silicon etch rate had been previously very good (see Figure 30) with PR mask but in this experiment at least oxide layer was etched unevenly. It is also interesting that with 50 % loading the etch rate of silicon had been greater on the edges of the wafer than on centre when PR mask was used (see Figure 30). Now the situation was completely reversed.

Combined depth of the remaining oxide layer and etched silicon was measured and it was found to be only around 7,5 microns compared with 30 μm when PR mask was used. Trench bottom was extremely rough. SEM pictures in the Figure 33 confirm the presence of the so-called black silicon. Pictures show also that profiles are positively tapered. According to SEM pictures, the height of BS is approximately 10 μm and the combined etch depth and BS height is roughly 15 μm.

7.3.2 Formation of black silicon

There are a few possible scenarios that could have led to formation of black silicon. The first one is that oxygen was released from the etched SiO_2 layer and the increased oxygen content of the process chamber led to overpassivation and resulted in black silicon. There are no previous reports in the literature that this could be the case. The second possibility is that the wafer had some kind of contamination on it and these particles acted as micromasks. This micromasking could also lead to formation of "grass". The wafers were just taken from the warehouse and cleaned carefully. Therefore it is highly improbable that contamination was the problem.

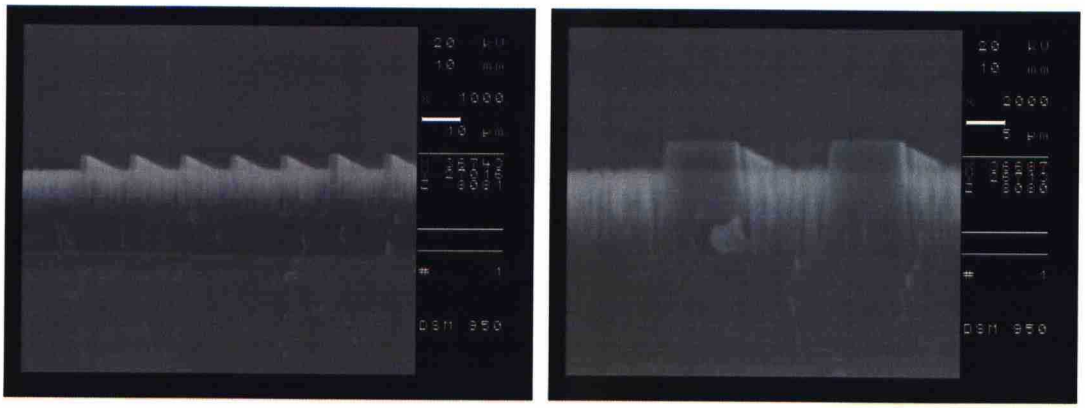
The third possibility is that lower helium flow and formation of black silicon had some kind of connection. As discussed in chapter 3.2.5, the function of helium backside pressure is to intensify the heat exchange between the wafer and cooled electrode. The clamping pressure controls the sealing of helium backside chamber. If one or the other parameter is changed it may result in different wafer temperature. Higher wafer temperature needs a higher amount of oxygen to form black silicon [41].

The pressure of the helium is fixed and it determines the flow rate of He. For some reason in this experiment the helium flow rate was lower than before. Lower helium flow indicates that sealing of helium backside chamber was better than previously

and that may have lead to lower wafer temperature. In lower temperatures less oxygen is needed to form black silicon [41].

In the experiments presented in chapters 4 and 5, the temperature of the wafer was probably not exactly the same as the temperature of the electrode but a little bit higher. Now, in this experiment the temperature exchange between the wafer and the electrode was more effective because of the better sealing of the helium backside chamber. Because other parameters remained unchanged lower wafer temperature could have been enough to initiate the forming of the black silicon.

The most probable reason to formation of BS is that in BHF etch the etch rate of oxide was lower than suspected. Therefore there was still a non-uniform residual oxide layer left on the wafer before DRIE of silicon. The oxide layer was slowly removed during etching process and when the silicon surface was reached the etch rate increased dramatically. The SiO_2 layer was not removed from all places exactly at the same time and that produced grass.



(a) (b)

Figure 33. Pillars that have black silicon between them. The wide pillars (b) have clearly positively tapered sidewalls.

7.4 TMAH etching

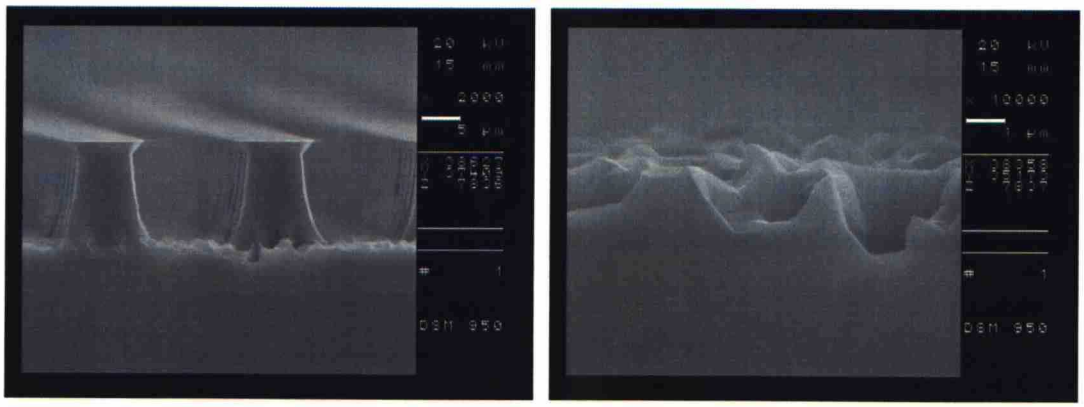
To make sure that the grass was really silicon and not some kind of sputtered polymer TMAH etching was performed. The etch rate of solid silicon in TMAH solution is around 400 nm/min but black silicon was etched faster because etching

cuts the long and narrow silicon spikes. This experiment ensures that grass on the bottom of the trenches was silicon.

Table 7. The effect of TMAH etching. The temperature of the TMAH solution was 84 °C.

Etch time	The colour of the sample	Measured etch depth
0 s	Black	7,5 μm
40 s	Grey	12,5 μm
70 s	Light grey	13,5 μm

SEM pictures of the Figure 34 are taken after TMAH etching. It can be seen that the surface of the silicon is still rough but there is no grass left. Undercutting and positive tapers can also be seen.



(a) (b)

Figure 34. (a) Pillars and grass after 70 seconds of TMAH etching. The oxide layer on top of the pillars can be seen. (b) Close up view from the trench bottom.

7.5 Etch rate of SiO_2

It is stated in the literature that etch rate of masking material is mostly dependent on CCP power but it does not have a big impact on etch rate of silicon [41]. To ensure this and to determine the ER of SiO_2 with different CCP powers another experiment was carried out. Three wafers with oxide masks were prepared and etched in same conditions, only CCP power was varied. The results of the experiment are presented in Table 8.

It can be seen that ER of silicon dioxide is strongly affected by CCP power, but ER of silicon hardly changes at all. Therefore the selectivity is also strongly dependent on CCP power. If the CCP power is too low the passivation layer on the bottom surface of the trench is not removed effectively and that leads to poor surface quality. In this experiment 1 W was slightly too low CCP power and bottom surface was not smooth.

Table 8. Etch rate of silicon and silicon dioxide in a function of CCP power. Selectivity between SiO_2 and silicon is calculated with equation {3}.

CCP power	Etch rate of silicon	Etch rate of SiO_2	Selectivity
1 W	3,1 μm / min	11 nm / min	280
2 W	3,2 μm / min	16 nm / min	200
3 W	3,2 μm / min	27 nm / min	120

8 Etch process optimization

As discussed in chapter 3.2, the change in one parameter may lead to completely different kind of etching result. Almost all previous experiments have been performed practically under same conditions. Etching results have been quite good with almost vertical sidewalls and smooth surfaces. The biggest problem has been slow etch rate. The purpose of the experiments presented in this chapter is to find a recipe that maximizes the etch rate and still profile, surface quality and selectivity have to be acceptable. Experimental results obtained will also be compared with theoretical trends.

8.1 The total gas flow and its influence on process pressure

One way to increase the ER is to use higher gas flows, but at the same time the process pressure should be maintained below 10 mTorr. Unfortunately low pressure and high gas flows are contradictory goals. Therefore it is important to determine, how high gas flows can be used without losing the ability to control pressure. To find out the relationship between the total gas flow and process pressure a simple experiment was carried out with the DRIE equipment. Dummy wafer was used and gas flows were changed during the etching and the minimum process pressure was measured. The results of the measurement are presented in the Figure 35.

Results show that when total gas flow is over 75 sccm the process pressure raises over 10 mTorr. If extremely good profile control and surface quality are needed, total gas flows over 75 sccm should be avoided.

Unfortunately the total gas flow is not always easy to control because of the helium leakage. It should be noted that besides backside pressure of helium, the helium leakage to the process chamber depends also on the wafer type and the clamping pressure. It was found out that the placement of the wafer inside the chamber is also crucial. If the wafer is not exactly at the right position, there is no seal between the backside cooling and the chamber. Therefore the helium leakage is high. The flat of the wafer causes extra leakage of helium to the chamber and therefore the wafer without a flat would be the most suitable choice. When using DSP wafers, the leakage to chamber is higher than with single side polished (SSP) wafer. If clamping

pressure is increased, helium flow to chamber degreases. The flows of the other gases can be accurately controlled with mass flow controllers.

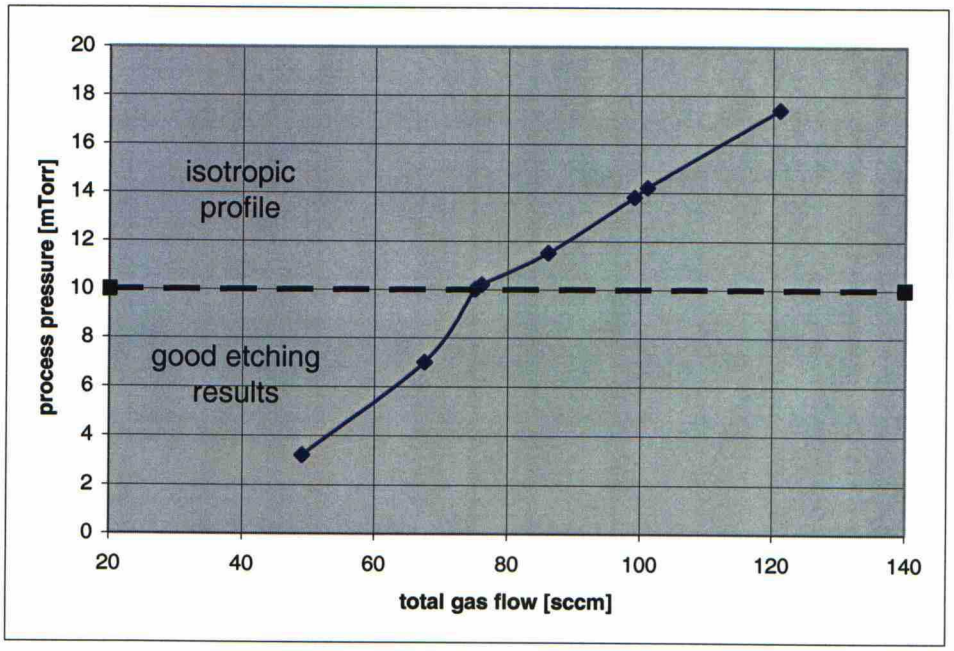


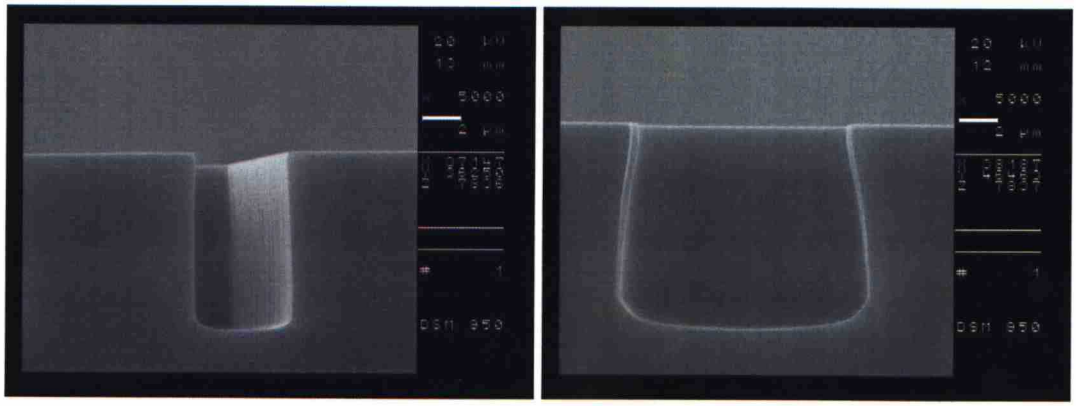
Figure 35. Process pressure in function of total gas flow. If the total gas flow into the chamber is higher than 75 sccm, 10 mTorr process pressure cannot be achieved.

8.2 Higher SF_6 flow

The goal of the experiment was to achieve higher etch rate. According to theory, it could be done by increasing the SF_6 flow if ICP power is high enough [41]. Process parameters and results of the baseline process and new process are presented in the Table 9. The ER of the new process was slightly higher than ER of the baseline process, but profiles were not as good as before. Process pressure was also slightly higher. In Figure 36 the trenches etched with the baseline process and new process are compared. All the trends are in accordance with the theory discussed in chapter 3.2.

Table 9. Process parameters and etch trends of the baseline process and new process. SF_6 flow is higher in the new process because higher etch rate is the goal. Higher total gas flow increased the process pressure.

	Baseline process	New process
Pressure	10 mTorr	11,3 mTorr
Temperature	-110 °C	-110 °C
ICP / CCP power	500 W / 3 W	500 W / 3 W
SF_6 flow	40 sccm	70 sccm
O_2 flow	6 sccm	6 sccm
Backside He pressure / flow	3-5 Torr / 5-10 sccm	4 Torr / 10 sccm
Etch time	7 min	7 min
Loading	50 %	50 %
Etch rate	1,6 μm / min	1,9 μm / min
Sidewall profiles	Almost vertical	Negatively tapered
Crystallographic dependence	No	Some



(a) (b)

Figure 36. A comparison of profiles etched with different process parameters. (a) The trench is etched with baseline process and the sidewalls are almost vertical. (b) The trench is etched with new process. Sidewalls are clearly negatively tapered even if the etched structure is quite large. Crystallographic dependece of etching can be seen at the trench bottom.

8.3 Higher SF_6 and O_2 flows

The next three wafers were etched with much higher total gas flows. Process parameters and etch rates are shown in the Table 10. Target pressure was 10 mTorr, but like shown in the chapter 8.1, the vacuum pump cannot maintain the low pressure

because of high gas flow rate. Like discussed in chapter 3.2.4, higher process pressure inflicts pronounced sidewall etching, bottling, undercutting and also crystallographic etching may appear.

Table 10. SF_6/O_2 flow rate ratio experiment. Measured etch depths, process pressures and profiles with different gas flows. Etching time is 7 minutes, temperature –110 °C, helium backside pressure 4 Torr, helium flow 9 sccm, ICP power 500 W and CCP power 3 W. All new processed led to crystallographic dependent etching.

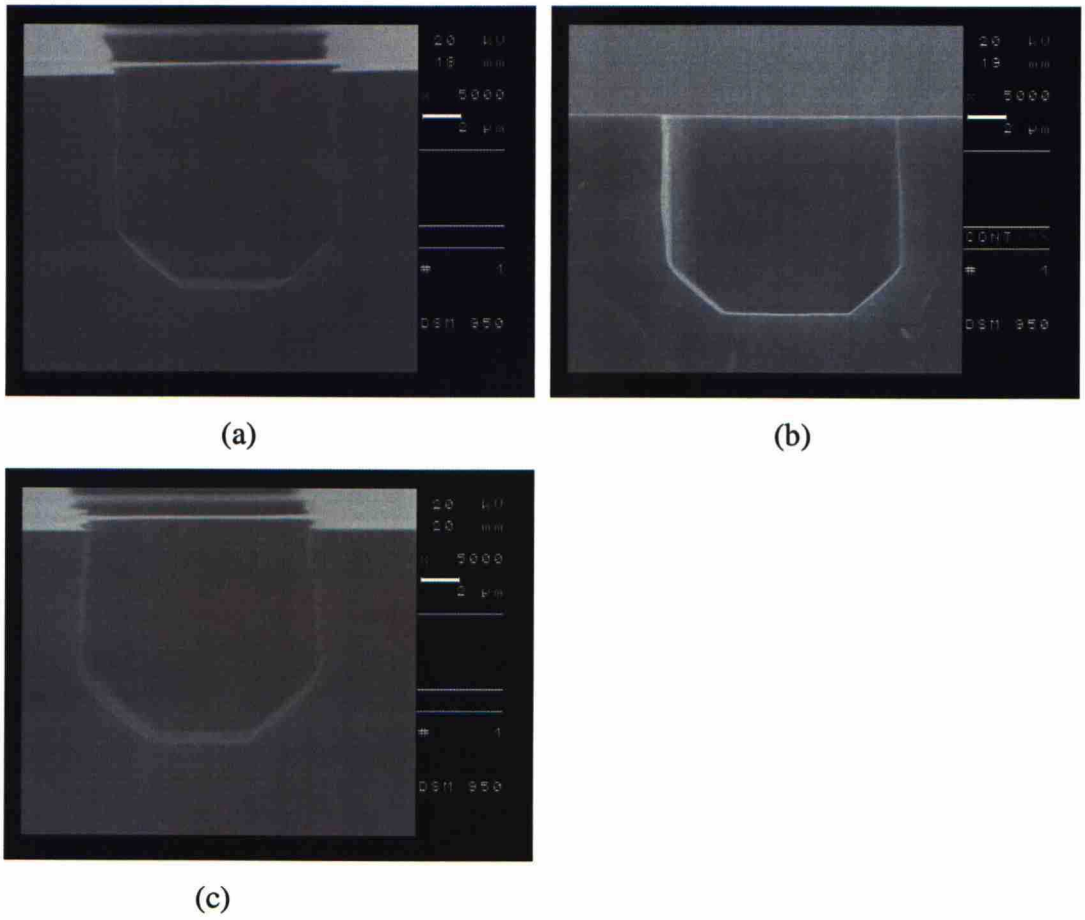
Process name	SF_6 flow	O_2 flow	Etch rate	Process pressure	Profile
Baseline	40 sccm	6 sccm	2,2 µm / min	10,0 mTorr	Vertical
Process A	80 sccm	10 sccm	1,8 µm / min	13,8 mTorr	Slightly negative
Process B	80 sccm	12 sccm	1,7 µm / min	14,2 mTorr	Almost vertical
Process C	100 sccm	12 sccm	1,8 µm / min	17,4 mTorr	Negative

Three SEMs in Figure 37 were all taken from the same structure but from the different wafers. Crystallographic etching can be seen in every case. This effect is most pronounced in Figure 37c because of the highest process pressure. Higher SF_6/O_2 ratio leads to more negatively tapered sidewalls. All these results are in accordance with theory.

Under the conditions of Table 9 the ER did not increase even if SF_6 flow was higher. The highest ER was obtained with smallest SF_6 flow. Increased supply of etchants did not result in higher etch rate because of ion angular distribution increased and ion bombardment was less vertical due to high process pressure. Collisions that ions experienced before hitting the surface also decreased the energy of the ions and led to crystallographic etching and reduced ER. The ER is at its maximum when conditions are near black silicon regime.

By increasing ICP power, the ER could be increased [41]. If ICP power is too low the increase of SF_6 flow does not have significant effect. By increasing the CCP

power it is possible to get rid of crystallographic dependent etching. The ER would also be slightly higher. Unfortunately higher CCP power hastens the ER of masking material substantially, as shown in the chapter 7.5.

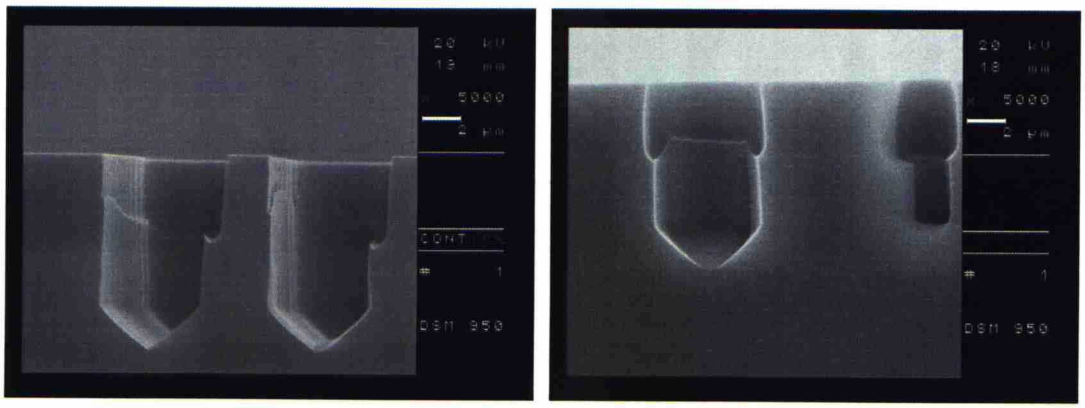


(a) (b)

(c)

Figure 37. SF_6/O_2 flow rate ratio experiment. (a) Process Test A: Silghtly negative sidewall profiles can be seen. Also a little bit of bottling in the upper part of the trench and clear crystal orientation dependend etching on the bottom suface. (b) Process Test B: Vertical sidewalls and clear crystal orientation dependend etching on the bottom suface. (c) Process Test C: Negative sidewall profiles can be seen. Also clear crystal orientation dependend etching on the bottom suface.

All unwanted effects that theory predicted could be found when gas flows were high and the process pressure over 10 mTorr. Directional defects right under the mask can be seen in the Figure 38a. This confirms that ion bombardment was not vertical because of higher process pressure. It can also be seen that slow etching planes meet on the bottom of the trench. Bottling can be seen clearly in the Figure 38b.



(a) (b)

Figure 38. Unwanted effects. (a) Process Test B: Defects appear right under the mask. (b) Process Test A: Bottling is very pronounced.

8.4 Maximizing the etch rate

The goal of this experiment was to maximize the ER of silicon. The selectivity and profile control were not as important and therefore also high process pressure and high CCP power were acceptable. This kind of process is needed for example when it is desirable to etch through the wafer. The parameters and the results of all the new processes are compared with baseline process in Table 11.

In long processes metal mask can be helpful because of its low etch rate. Therefore metal mask was used in Processes E and F. Aluminium layer whose thickness was 200 nm was sputtered on the wafers. Aluminium layer was patterned with the help of lithography and it was etched in phosphoric acid based solution. Then the photoresist was removed and the aluminium was sintered in 450 °C for 30 minutes. One of the wafers was not patterned. Patterned wafers were cut in small pieces and one piece was glued to non-patterned wafer with the help of phororesist. This way the loading and the consumption of the wafers were very small. Same carrier wafer was used in Process G.

To make the etch rates of different processes more comparable, loading compensated etch rates were calculated to baseline process and to Process D. This was made by proportioning measured etch rates to etch rate of the wafer whose loading was 2 % (see Table 3). Proportioning was made with equation {6}.

$$ER_{compensated} = \frac{ED_{2\%-loading}}{ED} * ER, \qquad \{6\}$$

where $ER_{compensated}$ is compensated etch rate; $ED_{2\%-loading}$ is the etch depth of the trench on wafer whose loading is 2 %; ED is the etch depth of the trench on the wafer whose ER will be compensated and ER is the etch rate to be compensated. The equation is valid only to wafers that have been etched for 7 minutes.

The surface quality of the trench bottom was good, the sidewalls were vertical and the undercutting small when using Process D (see Figure 39). This is because of the low process pressure and CCP power. Still the etch rate was high compared to baseline process.

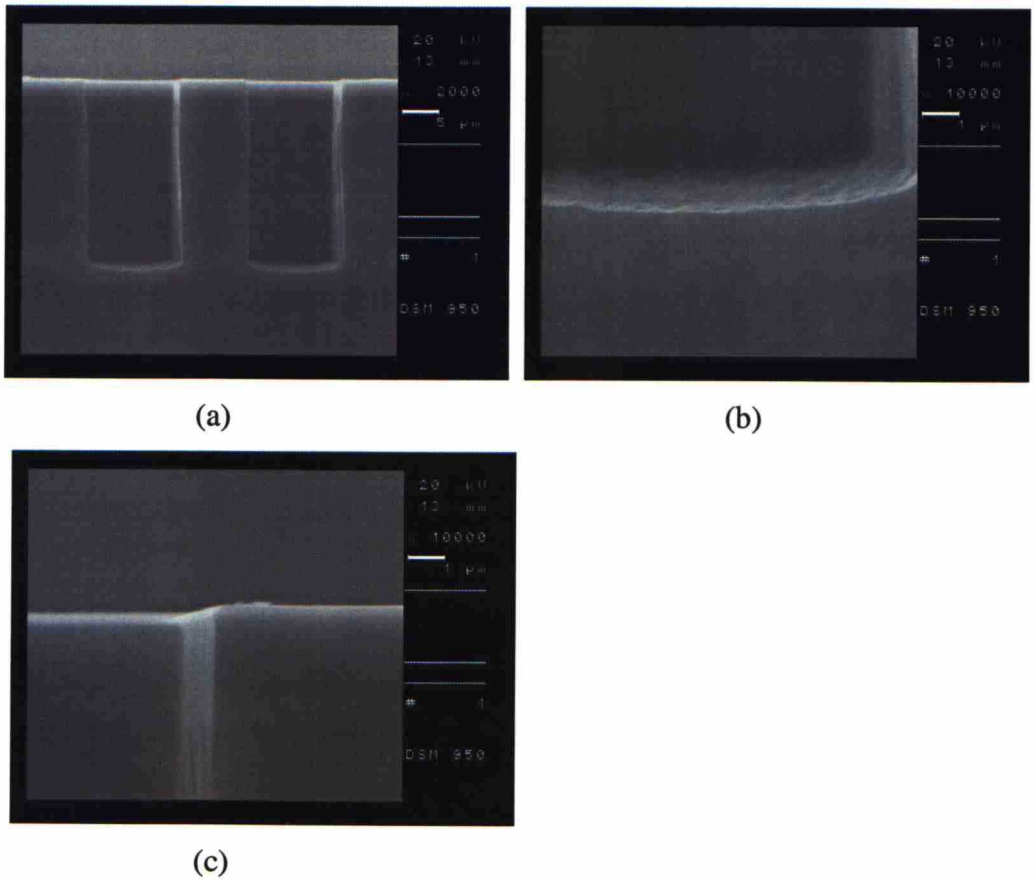


Figure 39. Etching results of the Process D. (a) Sidewalls are vertical. (b) The trench bottom is smooth. (c) The undercutting is small.

The Process F was used to etch through 300 μm thick wafer. After 59 minutes of etching 150 μm wide line was etched through from a few spots. To make sure that whole line was etched trough, 5 minutes over etching was performed. The average ER of the silicon was approximately 5 μm / minute. When etching only 7 minutes under the same conditions the etch rate was 5,6 μm / minute. It can be concluded that ER slowly decreases, as aspect ratio increases.

The Process G gave the highest etch rate. The profile of the structure was still quite good and the surfaces fairly smooth (see Figure 40). Undercutting was pronounced because of the higher process pressure, but the etch rate was over 7,6 μm/min. Etching was not dependent on crystallographic orientation even if the process pressure was high. This is probably because of the high ICP power.

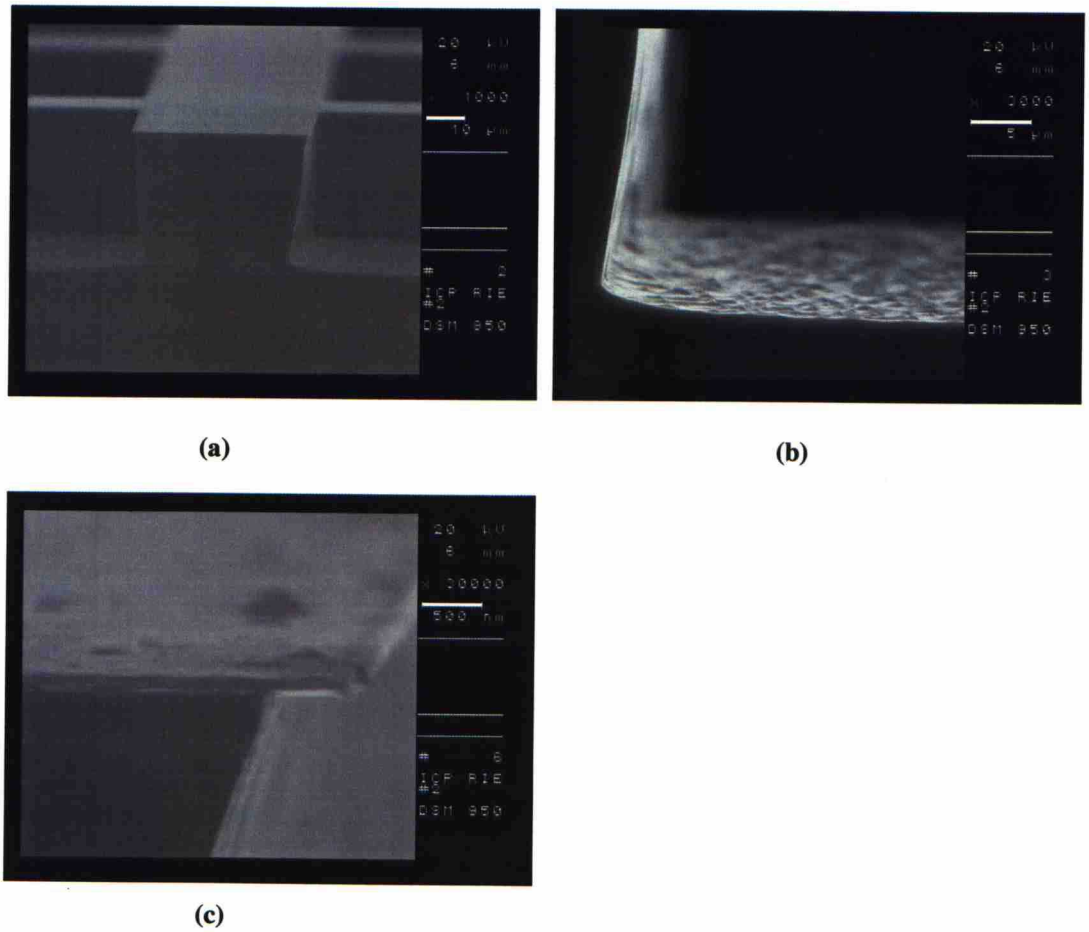


Figure 40. Etching results of the Process G. (a) The profile of the trench is quite good. (b) The bottom of the etched trench is also fairly smooth. (c) Pronounced undercutting. Photo courtesy to Kestutis Grigoras, Helsinki University of Technology.

Table 11. Etch rate maximization experiment. Four new processes compared with baseline process. The highest etch rate is achieved when using high ICP power and gasflows, but the ability to control the process pressure is lost. CCP power is has no significant effet to ER. All the processes have 5 Torr heluim backside pressure. Helium flow to the chamber is under 10 sccm.

	Baseline process	Process D	Process E	Process F	Process G
Pressure [mTorr]	10	10	10	15,5	19,5
Temperature [°C]	-110	-110	-110	-110	-110
ICP / CCP power [W]	500 / 3	1000 / 3	2000 / 8	2000 / 30	2000 / 3
SF_6 flow [sccm]	40	40	50	80	100
O_2 flow [sccm]	6	6	6	12	15
Etch time [min]	7 min	7 min	7 min	7 min	5 min
Loading [%]	50 %	11 %	~1 %	~1 %	~1 %
Etch rate [μm / min]	1,6	4,3	3,8	5,6	7,6
Calculated loading compen. ER [μm / min]	2,6	4,9	-	-	-
Sidewall profiles	Vertical	Vertical	Vertical	Negative	Negative
Crystallographic dependence	No	No	No	No	No
Masking material	PR	SiO_2	Al	Al	PR
Glued to carrier wafer	No	No	Yes	Yes	Yes

In the Process G, ICP power was now only 1,5 kW. The etch rate of silicon was still well above 7 μm / minute. Therefore it can be concluded that the limiting factors of ER are the supply of the fluorine and the poor efficiency of the vacuum pumps. At these conditions the SF_6 flow affects directly on etch rate. Maximum SF_6 flow of our system is 100 sccm, but it cannot be used if perfectly anisotropic etching result is needed.

9 Fabrication of the capillary chip

In this section the fabrication of lidless capillary filling chips that were briefly discussed in chapter 2.4 is discussed. The first step of the fabrication process was the drawing of the lithography mask. Mask designing program CATENA Layout Editor LAYED was used. Ten different chips were drawn and one of them is shown in Figure 41.

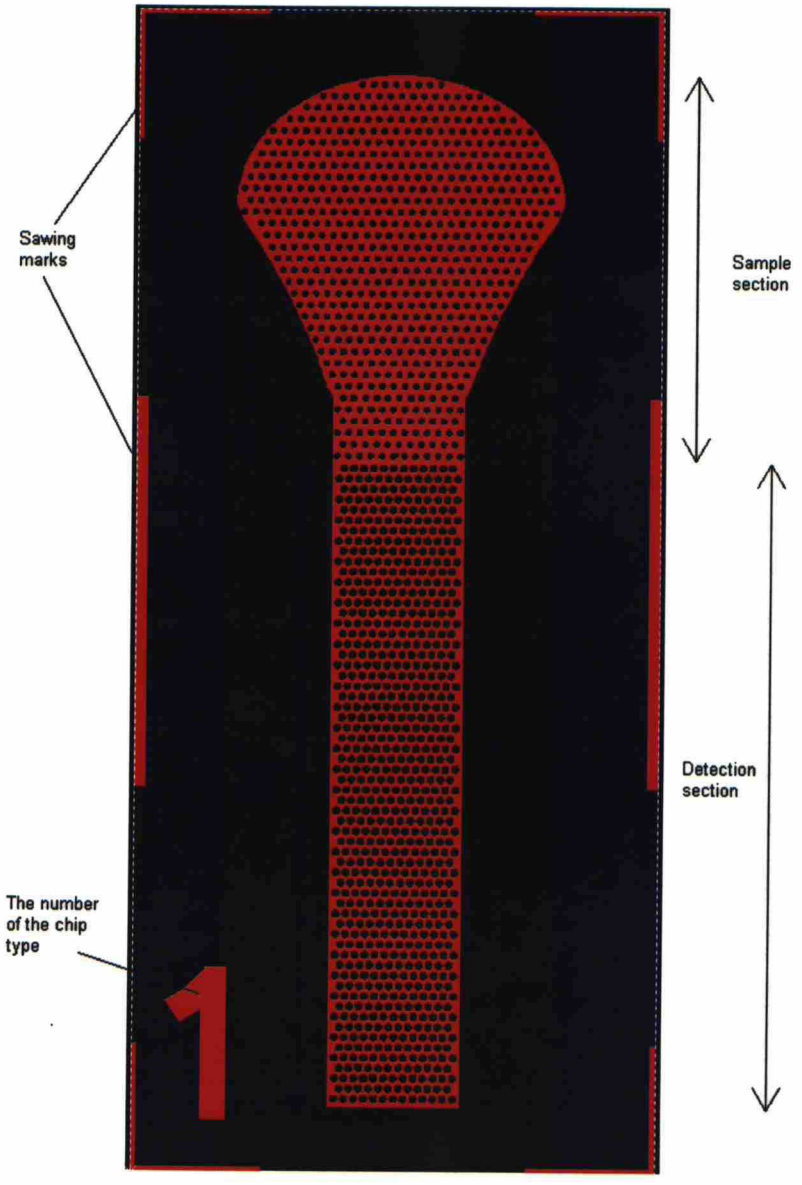


Figure 41. One of the ten capillary filling chips designed. Red is the area that will be etched away and black area will be protected. The liquid is deposited to the sample section of the chip and it flows through the detection capillary. The list of the parameters of all ten chips is represented in detail in appendix 1.

All of the chips have overall dimensions of 20,25 mm x 9 mm. The chips have two different sections as shown in the Figure 41. The sample is inserted into the sample section that has larger pillar spacing than the detection section. Therefore the flow in the sample section is slower. The pillar diameter of the sample section is also smaller than the pillar diameter of the detection section. The complete listing of dimensions of the chips is represented in appendix 1. All of the chips have sawing marks on the edge of the chip and identification number on the lower left corner of the chip.

All ten different chip types were tested. The purpose of the experiment was to investigate how the changes in

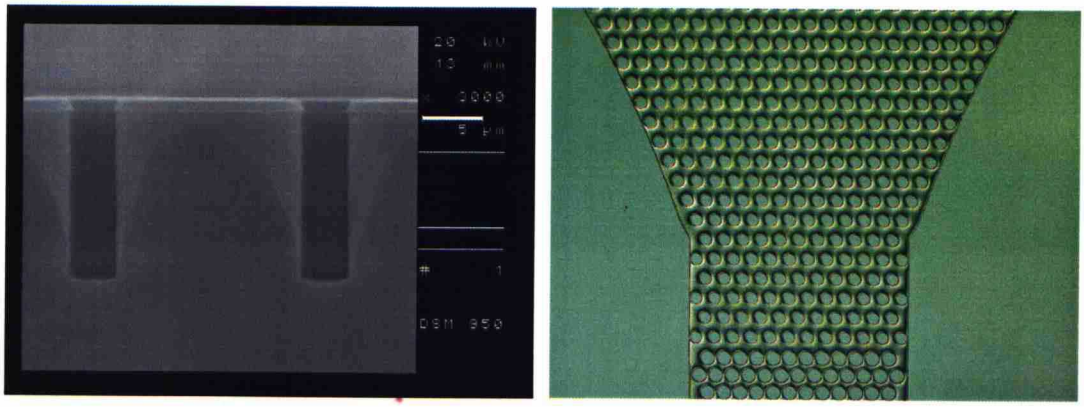
- pillar shape
- pillar size
- pillar spacing
- detection channel width

influence the sample flow. One of the ten chips was fabricated according to simulation results made by Vervoort and his co-workers [11]. Simulation results are also presented in chapter 2.2.2 of this thesis. The other parameters under study were the distance between the sidewall and the first pillar row and the depth of the channel.

9.1 Fabrication process

The fabrication process of the capillary filling chips was straightforward. Lithography step that defined the channels was made to three silicon wafers and the wafers were etched. Process parameters of the Process D of the Table 11 were used, with the etching time of 14 minutes. This resulted in 42 μm deep channels. The bottom surfaces of the channels were a bit rough after etching.

Photoresists were removed from two wafers. Then, one was treated in oxygen plasma for 90 seconds and the other wafer was washed in RCA-1 bath for 10 minutes. In both processes a thin SiO_2 layer grows on the wafers and makes the surfaces hydrophilic. Nothing was done to the last wafer after etching and therefore it remained hydrophobic.



(a) (b)

Figure 42. Capillary filling chip after processing. The heights of the pillars in the picture are 21,8 μm. (a) Cross-sectional SEM picture of the round pillars. Pillar walls are smooth and verical. (b) Top view of the chip taken with optical microscope.

9.2 Capillary filling measurements

The first capillary filling experiments were done inside the clean room right after etching. A droplet of de-ionized (DI) water was pipetted to sample section of the chip (see Figure 41) and the flow of the water was observed with an optical microscope. The volume of the droplet was several microliters. It could be seen that water moved inside the capillary. The speed of the waterfront was not uniform. It moved by jumps from one pillar row to another. The average speed was quite slow. The fastest flow was obtained with chip number 10 that was completely filled after two minutes. Pillar density of the chip number 10 was highest. The detection section of the chip has pillars whose diameters are 33,75 μm. Lateral space between two the pillars is 7,88 μm and vertical space is 2,25 μm. Detection channel has the width of 2,25 mm and the length of 5,07 mm.

The same experiment was done right after photoresist removal and it was found out that water did not flow through the channel anymore even if the wafers were carefully rinsed after the acetone and isopropyl alcohol treatments. This indicates that after etching there is some kind of residual layer on the silicon. It cannot be the SiO_xF_y layer because it is mostly evaporated during the warming to room temperature. The residual film is removed in PR removal process and the surface becomes more hydrophobic.

The experiment was repeated to the first wafer after the oxygen plasma treatment and to the second wafer after the RCA-1 clean. Both wafers behaved exactly the same way after these treatments. All the 10 channel designs filled almost instantly when the droplet hit the surface. This is because both of the treatments created a thin SiO_2 film on the wafer.

The same experiment was done two days later outside the clean room with an accurate pipette. The volume of the droplet was 2 µl. All the channels that had been made hydrophilic filled almost instantly when the droplet was pipetted to the sample section. When using the untreated hydrophobic chips, the only chip design that worked was number 10. The filling of the channel took few minutes. The hydrophilic chips showed also promising properties in transporting fluorescent markers.

It can be concluded that micropillars initiate capillary flow as expected. The spacing between the pillars is an important factor when considering the flow rate. Smaller spacing results in faster sample flow. Still, the flow rate is mostly defined by the hydrophilicity of the channel surface as the equation {2} suggests. Pillar shape or detection channel width did not seem to have remarkable effect. The depth of the channel defines the maximum sample volume that can be used.

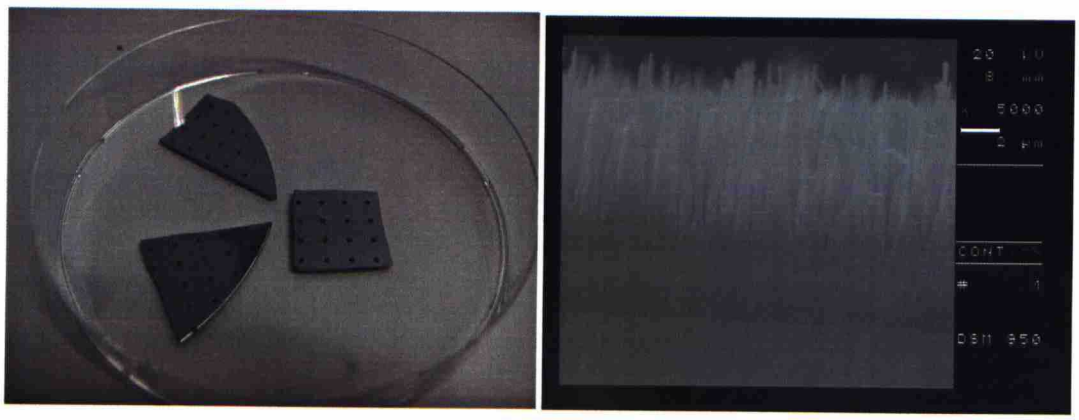
10 DIOS-MS with black silicon sample plate

In this chapter the use of black silicon as a sample plate material in desorption / ionization on silicon mass spectrometry (DIOS-MS) is demonstrated and the results are compared with the results obtained from porous silicon plate. Various compounds were tested and the measurements were done with matrix-assisted laser desorption ionization mass spectrometer (MALDI-MS) instrument.

10.1 Fabrication of black silicon

As discussed in chapter 3, overpassivation during the cryogenic etching process initiates formation of black silicon (BS). Therefore the fabrication of BS is straightforward unlike the fabrication of porous silicon that requires electrochemical etching. BS and porous silicon are quite similar materials. Because of the easier fabrication process of BS it would be beneficial to replace porous silicon with BS.

Round 1 mm areas of BS were fabricated on a silicon wafer because of suitable evaporation pattern [23]. These areas were defined with standard lithography step. The etching was done in a single 7 min step. Process D of Table 11 was used, but the oxygen flow was raised from 6 sccm to 18 sccm, to initiate the formation of BS. The pictures of black silicon are shown in the Figure 43.



(a) (b)

Figure 43. Pictures of BS. (a) Pieces of silicon wafer where BS can be seen as black spots. Photo courtecy to Laura Luosujärvi and Tiina Sikanen, Helsinki University. (b) Cross sectional view of BS taken with SEM, after ICP-RIE.

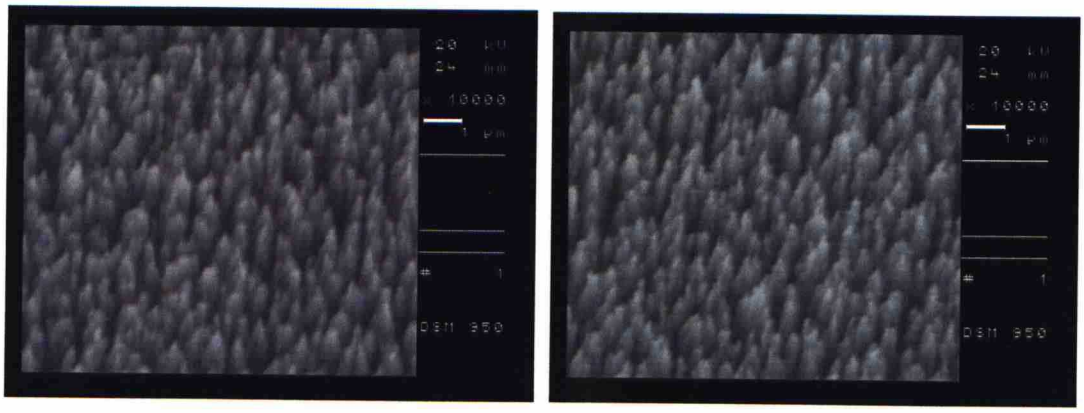
10.2 DIOS-MS

10.2.1 Preparation of sample plate

Before applying the liquid sample, a preparation step was performed to the BS sample plates. Three different preparation procedures were tested and their effects to the results were studied. Preparation steps are:

1. EtOH rinsing just before the experiment. The purpose of rinsing was to clean the surface of BS from loose particles.
2. 10 – 20 s dip in HF:EtOH (1:1) solution and rinsing in H_2O:EtOH (1:1) solution just before experiment. The purpose of HF treatment was to remove native oxide from the surface.
3. Over 1 min HF:EtOH (1:1) bath and rinsing in H_2O:EtOH (1:1) solution just before experiment.

The previous experiences with porous silicon sample plate show that HF treatment before experiments makes the intensity of the mass spectrometry signal higher and it also reduces the background noise. To make sure that HF treatment did not harm the BS, SEM pictures were taken before and after the HF treatment (see Figure 44).



(a) (b)

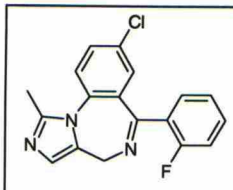
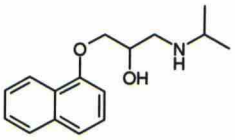
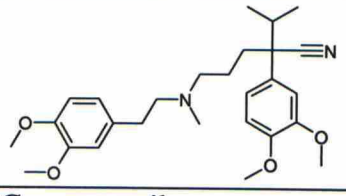
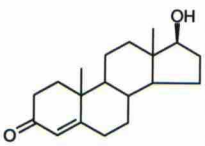
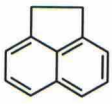
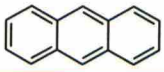
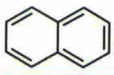
Figure 44. Tilted top view SEMs of the BS (a) before and (b) after the HF treatment. HF treatment does not change the BS structure.

10.2.2 Sample application

The test compounds used in DIOS-MS experiments are presented in Table 12. Sample dilutions of 500 μM were made from the compounds and they were applied

on black silicon spots on the wafer. Two 0,2 µl droplets were pipetted and evaporated. This means that amount of test compound on the sample plate was 200 pmol.

Table 12. Test compounds that are used in DIOS experiments.

			
A: midazolam	B: propranolol	C: verapamil	D: testosterone
			
E: acenaphthene	F: anthracene	G: naphthalene	

10.2.3 Results and conclusions

Compounds A-D could be detected with DIOS-MS but compounds E-G could not be detected. These three could not be observed with porous silicon sample plate either. A clear difference between pre-treatments could not be made because the intensity of the laser was changed during the measurements. The mass spectrum of midazolam is presented in Figure 45. $[M+H]^+$ ions can be observed, but also adduct ions $[M+Na]^+$ and $[M+K]^+$ are clearly present. When comparing the signal intensity obtained from porous silicon and BS sample plates the BS plate was superior, but adduct ions were not a problem when porous silicon sample plate was used.

Adduct ions are most likely originated from the fabrication process of the BS. Developer solution of photoresist contains sodium. By adding a few cleaning steps before starting the process the quantity of adduct ions could be decreased substantially. SiO_2 mask should be used instead of PR. This way silicon surface would not be in direct contact with developer solution of PR.

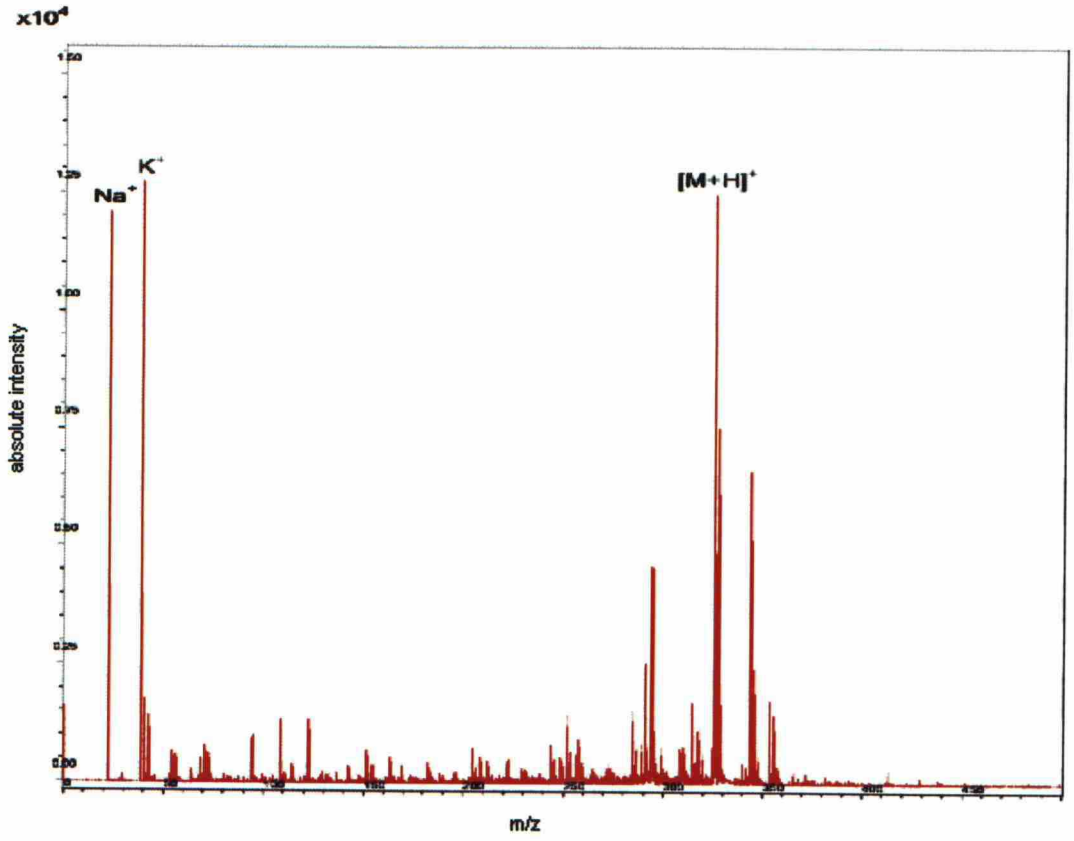


Figure 45. A mass specrum of midazolam on BS sample plate. Pre-treatment 2 was made before the sample application. Besides $[M+H]^+$ ions, also $[M+K]^+$ and $[M+Na]^+$ adduct ions can be seen clearly. Spectrum courtesy to Tiina Sikanen and Laura Lousujärvi.

These first results show that black silicon has potential to replace porous silicon as DIOS-MS sample plate material. BS has all the same good qualities as porous silicon and the added benefit of easy fabrication process. By changing the process flow of BS, the adduct ion problem can most likely be solved. The properties such as diameter and height of BS peaks can be changed by changing the process conditions [33]. This makes possible to optimize the properties of the sample plate.

11 Conclusions

Cryogenic DRIE equipment for silicon etching was characterized. It was found out that the general guidelines given in the literature [37, 41] are valid also for our reactor. The maximum etch rate obtained was observed to be approximately 7,6 μm/min that is almost two times more than the 4 μm/min etch rate promised by manufacturer of the equipment. Etch rate is mostly determined by ICP power and flow rate of SF_6. If slightly lower etch rate is acceptable extremely smooth and anisotropic etch result can be attained.

Loading and microloading effects could be seen clearly. The etch rate of silicon is affected crucially by loading. The etch depth of trenches on wafer with 50 % loading was only 62% of the etch depth of the trenches that were on the wafer with 2 % loading. Also the sidewall angles are loading dependent. The radial uniformity of the etched wafers was excellent.

The selectivity of the masking material was found out to be strongly dependent on CCP power. With low CCP power the selectivity between SiO_2 and silicon was almost 300, but it decreases quickly when CCP power increased. Aluminium mask has almost infinite selectivity and therefore it is good masking material in through wafer etching processes. Photoresist has lower selectivity than silicon dioxide and it may also crack in low temperatures. Especially thick PR layers are prone to cracking. Photoresist cracking is poorly studied phenomenon, but the experiments presented in chapter 6 strongly suggest that helium backside pressure plays an important role in PR cracking process and therefore high backside pressures should not be used with PR mask. Surprising result was that SU-8 resist did not have any cracking problems. Even over 70 μm thick SU-8 layer was unharmed after etching process.

After characterization of the cryo-DRIE equipment, it was utilized for the fabrication of lidless capillary filling chip. Capillary forces move the liquid inside the channel because of dense micropillar array etched on the bottom of the channel. Dense pillar array leads to fast liquid flow in the channel. In less dense channel the flow is slower. Lidless channels are very useful because their fabrication process is simple and fast. The other great advantage is that application and detection of the sample is very easy.

The development of capillary filling chip will continue. Objective is to create higher surface-to-volume ratio channels that are capable to liquid chromatography.

Over passivation during the etching process results in formation of black silicon. BS has large surface to volume ratio and it also absorbs light in UV range. It was demonstrated that BS could be used as sample plate material in DIOS-MS. Until now porous silicon has been the sample plate material. BS may replace porous silicon because of its extremely easy fabrication process. In the near future adduct ion problem of the black silicon will be solved. Also the influence of etch parameters on the properties of black silicon will be studied. The goal is to maximize the signal intensity obtained from BS.

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Appendix 1: Parameters of the capillary filling chips

Parameters of the chips that have round pillars

Parameters	Chip 1	Chip 2	Chip 5	Chip 6	Chip 7	Chip 8	Chip 9	Chip 10
The shape of pillars	Round	Round	Round	Round	Round	Round	Round	Round
The diameter of the sample section pillars	112,5 µm	56,25 µm	168,75 µm	112,5 µm	112,5 µm	56,25 µm	135 µm	33,75 µm
The horizontal distance between sample section pillars	78,75 µm	43,75 µm	118,13 µm	78,75 µm	78,75 µm	112,5 µm	56,25 µm	15,75 µm
The vertical distance between sample section pillars	90 µm	45 µm	135 µm	90 µm	90 µm	123,75 µm	67,5 µm	4,5 µm
The distance between the first pillar row and sidewall in sample section	16,88 µm	21,38 / 20,81 µm	36,56 µm	16,88 µm	67,5 µm	16,88 µm	5,63 µm	6,75 µm
The diameter of the detection section pillars	135 µm	67,5 µm	202,5 µm	135 µm	135 µm	101,25 µm	157,5 µm	33,75 µm
The horizontal distance between detection section pillars	33,75 µm	16,88 µm	50,63 µm	33,75 µm	33,75 µm	67,5 µm	11,25 µm	7,88 µm
The vertical distance between detection section pillars	45 µm	22,5 µm	67,5 µm	45 µm	45 µm	78,75 µm	22,5 µm	2,25 µm
The distance between the first pillar row and sidewall in detection section	45 µm	15,75 / 15,19 µm	74,48 µm	45 µm	45 µm	45 µm	33,75 µm	5,06 µm
The width of the detection channel	2250 µm	2250 µm	2250 µm	1575 µm	2925 µm	2250 µm	2250 µm	2250 µm
The distance between the sample and detection sections	90 µm	90 µm	135 µm	90 µm	90 µm	90 µm	67,5 µm	11,25 µm
The channel length of the sample section	1080 µm	1080 µm	1080 µm	1080 µm	1080 µm	1080 µm	1080 µm	1098 µm
The empty space at the end of the detection cha.	90 µm	67,5 µm	22,5 µm	90 µm	180 µm	90 µm	157,5 µm	135 µm

Parameters of the chips that have diamond shaped pillars

Parameters	Chip 3
The shape of pillars	Diamond
The length of side of the sample section pillars	90 μm
The horizontal distance between sample section pillars	74,25 μm
The vertical distance between sample section pillars	74,25 μm
The distance between the first pillar row and sidewall in sample section	49,94 μm
The length of side of the detection section pillars	101,25 μm
The horizontal distance between detection section pillars	32,63 μm
The vertical distance between detection section pillars	32,63 μm
The distance between the first pillar row and sidewall in detection section	43,88 μm
The width of the detection channel	2250 μm
The distance between the sample and detection sections	73,13 μm
The channel length of the sample section	1080 μm
The empty space at the end of the detection channel	22,5 μm

Parameters of the chips that have honeycomb shaped pillars

Parameters	Chip 4
The shape of pillars	Honeycomb
The maximum length of honeycomb of the sample section pillars	135 μm
The maximum width of honeycomb of the sample section pillars	90 μm
The horizontal distance between sample section pillars	78,75 μm
The vertical distance between sample section pillars	90 μm
The distance between the first pillar row and sidewall in sample section	33,75 μm
The maximum length of honeycomb of the detection section pillars	135 μm
The maximum width of honeycomb of the detection section pillars	90 μm
The horizontal distance between detection section pillars	33,75 μm
The vertical distance between detection section pillars	33,75 μm
The distance between the first pillar row and sidewall in detection section	28,13 μm
The width of the detection channel	2250 μm
The distance between the sample and detection sections	90 μm
The channel length of the sample section	1080 μm
The empty space at the end of the detection channel	101,25 μm